# NE 445L/471 Nano-Electronics Lab Report

##

University of Waterloo
4A Nanotechnology Engineering
Group 7

#### Rajesh Swaminathan Student ID: 20194189Lab Partner: Peter Lee (20201956)

 **Dates Lab Performed On:** Nov 17, Nov 24, Dec 1
**Lab Report Submitted** on Dec 3 2009
**Lab Instructor**: Rossi Ivanova
**Lab TA**: Sepehr Forouzanfar

### Lab Objective

The primary objective of the NE 471 laboratory is to learn how to design a MEMS device using software and to be able to evaluate and verify the feasibility of this design using a modelling program, namely COMSOL multiphysics. In doing so, we learn how to design actual masks for each layer of the MEMS device by incorporating the various established design rules. The devices designed in this term will be fabricated next term in the Winter. This laboratory provides a comprehensive introduction to the simulation of complex designs on COMSOL and also introduces us to the LayoutEditor MEMS design software.

We designed masks for 3 designs. The following sections explain these designs and provide verification for them through modelling on COMSOL multiphysics.

**Design #1 – MEMS Capacitor**

The first design was a simple MEMS capacitor setup similar to that outlined in the lab manual.



Figure 1 Simple MEMS Capacitor Layout Designed Using LayoutEditor



Figure 2 Zoomed in version of

This capacitor comprises of a 0.08 m layer of chromium first (green mask), then a 0.3 m layer of SiN deposited by PECVD (blue mask). The third mask (red) contains the design for a release layer made of photoresist to be etched away later. The final mask (lime green) provides the Aluminum contacts for the capacitor. This layer also has many holes in it to allow the etchant to go through the aluminum and etch off the photoresist layer.

The resulting structure is a MEMS capacitor with an aluminum layer over a chromium layer with an air gap in between. As a potential is applied on the aluminum contacts, the upper aluminum layer bends due to electrostatic interaction and reduces the air gap between the chromium and aluminum layers. This in turn increases the capacitance between the air gap.

This design was modelled on COMSOL multiphysics to verify its feasibility. The following surface profile plot () for the total displacement experienced by the top aluminum arm of the capacitor.

This layout was modelled in COMSOL. This is how our model in COMSOL looked like:



The surface plot is shown below:



Figure 3 COMSOL modelling results showing surface plot for the total displacement of a simple MEMS cantilever

As we can see above, not much bending of the cantilever is observable. But if we applied more voltage, more bending would be observed.

We plotted the total displacement of the membrane as a function of the voltage:



Finally, we plotted capacitance as a function of potential:



**Design #2 – MEMS Cantilever**

The layout for a double MEMS based cantilever is shown below in .



Figure 5 Double MEMS based cantilever layout

The cantilever has 4 aluminum contact bases. Applying a voltage on the top and bottom contact bases causes the contacts to warm up and expand. However, the cantilever is held in place on the sides by the four aluminum contact bases. Thus the expansion of the cantilever will cause it to bend upward by a predictable amount. Since this device is symmetric across the x-axis, the bending will form a triangle. Measuring the amount of this bending will give us a measure of the amount of voltage applied at the contacts.

Due to the complexity of this layout, this design was *not* modelled in COMSOL.

**Design #3 – Thermal Gate**

Our last design was a thermally actuated gate on the micro scale. The mask layers for this design are shown below:



This design only has two layers. A sacrificial photoresist layer that will be eventually removed, and an aluminum layer on top of it. The way this device works is that a potential applied to the two top contacts heats up the area around it. This heat travels downwards through the legs, but the expansion will be more in the narrower leg than in the wider one because the wider leg has a larger surface area and therefore a larger sheet resistance.

Since the two legs expand by different amounts, and because the two legs are connected at the bottom, this will cause the entire structure to bend leftwards to touch the aluminum gate on the left. Consequently, a potential will be detected on the bottom-left contact. Thus, the device is working like a thermal gate where a potential will be detected on the bottom-left contact only if a sufficient potential difference is applied on the top two contacts to cause the legs to bend to a sufficient amount. Our gap between the legs and bottom-left contact is 20 m:



# We simulated this model on COMSOL multiphysics to verify its feasibility. The COMSOL model layout looked like this in 3D:



The surface plot for the total displacement is shown below:



It can be seen from the above surface plot that the maximum displacement at the end of the cantilever is 35 m. Since our gap between the legs and bottom-left contact is 20 m, we can be guaranteed that the legs are bound to touch the bottom-left contact and closing the circuit.

# References

[1] R. Ivanova, Nanotechnology Engineering NE 454L/471L Nanoelectronics Lab Manual, Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Sep 2009.