Si/Ge Nanowires as High Performance FETs

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Why semiconducting nanowires?

Semiconductor *nanowires* are potential alternatives to conventional planar (MOSFETs). Nanowire FETs (NWFETs) have a unique electronic structure which we can try and exploit. Carriers in nanowires have longer mean free paths and are subjected to reduced scattering thanks to one-dimensional quantum confinement effects. Unlike carbon-nanotubes (CNTs), the electronic properties of nanowires are highly reproducible in a large-enough yield required for VLSI systems and applications. In ref. [1], a nanowire based FET using high-k dielectrics in a top-gate geometry was reported (Fig. 1a,b,c). This FET displayed enhanced gate coupling, and a scaled transconductance ($\partial I/\partial V$) and "on" current that was three to four times greater than state-of-the-art MOSFETs. Furthermore, the intrinsic switching delay τ substantially exceeded values obtained in planar silicon MOSFETs.

Silicon and germanium nanowires have been studied for a few years but Schottky barriers and scattering from charged dopants have always limited intrinsic mobility and device performance. Lieber et al [1] have demonstrated transparent contacts and low-bias ballistic transport with *undoped* Ge/Si core/shell nanowire heterostructures. These heterostructures have a mean free path as high as 500 nm. Further, enhanced mobility is observed due to reduced scattering and since not one, but several sub-bands may participate in NWFET transport.

What performance benefits were observed?

In reference [1], NWFET high-performance devices using thin HfO_2 and ZrO_2 high-k gate dielectrics were fabricated (Fig. 1d,e). The family of $I_d - V_{ds}$ (Fig. 3a) curves show that the drain current I_d first increases then saturates with increasingly negative drain voltage, similar to a conventional long channel MOSFET. The authors have demonstrated that the device has a peak transconductance, $g_m = dI_d/dV_g$ of 26 μS. The device exhibits a maximum drain current $I_{d(max)}$ of 35 μA at V_g = -2 V. The authors note that these values of g_m and $I_{d(max)}$ substantially exceed the best performance

reported to date in single semiconductor NWFETs. Because the geometric gate capacitance per unit area is only 29% larger than that of conventional Si p-MOSFETs, the large increase in g_m and I_{on} cannot be accounted for by an increase in gate capacitance alone. The hole mobility for this fabricated Ge/Si NWFET is more than ten times better than that of the Si p-MOSFET. The above improvements are attributed to the quasi-1D transport in clean Ge/Si heterostructure nanowires.

Furthermore, no significant short-channel effects were observed for devices down to at least $L =$ 190 nm. In general, an FET with a small S is essential for modern logic circuits as it reduces the "off" state current and therefore minimizes static power dissipation.

Data obtained for the fabricated NWFET show a clear speed advantage at a given L: the intrinsic delay $\tau = CV/I$, where C is the gate capacitance and I is the "on" current, for a 190 nm Si planar device is larger than 10 ps (picoseconds), but this is about *three* times longer than the intrinsic delay obtained in the Ge/Si NWFET. This considerable difference is attributed to the suppression of scattering in the quasi-1D quantum confined Ge/Si nanowires.

The authors have tweaked the design of their NWFET slightly and come up with an asymmetric gate structure (Fig. 5b) to suppress ambipolar conduction which limits the maximum on/off ratio that can be reached. The new gate design was able to tune the threshold voltage V_T through the gate metal *work function*. Optimal device operation is critically dependent on how well V_T can be controlled, and therefore tunability is easily achievable through a choice of top gate metal with specific work function in fabrication.

It is well known that Schottky barriers exist at CNT contacts. However, such limitations do not exist for Ge/Si NWFETs which do not have contact barriers, and thus the asymmetrical gate structure can yield unipolar NWFETs without sacrificing performance.

What challenges were encountered and how were they addressed?

Two major challenges were encountered with the performance of the NWFET. First, a non-ideal gate coupling ($\alpha < 1$) was observed which yielded a larger S value since $S \propto 1/\alpha$. This, according to the authors, was due to a finite trap state density at the nanowire/high-k interface. Optimizing of the deposition process of the oxide layer during fabrication should yield improved interface quality and enable ideal sub-threshold behaviour.

The second challenge encountered was that of ambipolar conduction, i.e. conduction by electron carriers (as opposed to holes). This type of conduction is detrimental to high-performance applications as it reduces the window of operation and increases the minimum off-state current. This issue was addressed with asymmetrical partial gates (Fig. 5b). More importantly, switching the source and drain electrodes dramatically suppressed the ambipolar current from 300 to 0.8 nA at V_{ds} = -1 V.

The physics of the above results can be explain as following: in the first case, electron injection at the drain increases with increasing V_g and ultimately dominates the current, while in the second case, the ungated region near contact 2 acts as a thick barrier to electron transport and suppresses electron current *even* at large downward bending of the conduction band.

What design issues did the authors come across?

A minor design issue that was mentioned is that the above fabricated Ge/Si NWFETs are *depletion-mode* devices with threshold voltage $V_T > 0$, and require $V_g > V_T$ to be turned off. *Enhancement-mode* FETs with $V_T < 0$ are technologically more desirable because they consume less static power.

What were the author's conclusions?

In summary, top-gated Si/Ge NWFET heterostructures with high-k dielectrics exhibit scaled transconductance and on-current values of 3.3 mS μm^{-1} and 2.1 mA μm^{-1}, respectively, which are *three to four times* greater than those for state-of-the-art MOSFETs. Hole mobility for Ge/Si based NWFETs is more than a factor of *ten* greater than the Si *p*-MOSFET with HfO_2 gate dielectric and more than *twice* that of Ge and strained SiGe heterostructure PMOS devices. Si/Ge NWFETs have demonstrated control over threshold voltage V_T as well as ambipolar behaviour. Further performance improvements can be brought about by optimizing gate coupling and size scaling. Thus Si/Ge nanowire FETs offer substantial promise for its use in high-performance applications. NWFETs could, in a few years, open up great advances in areas of application such as high-frequency electronics on plastic and glass substrates, highly sensitive nanosensors, and possibly high-performance logic and computation.

How can high-speed electronics be made on plastic and glass substrates?

Large-scale integrated circuits made on substrates of glass and plastic could be prove to be very advantageous because of their light weight, high flexibility and low cost. Unfortunately, these glass and plastic substrates deform at high temperatures so, until now, only semiconductors such as organics and amorphous silicon could be used, leading to poor performance. The authors in [2] present a low-temperature process to integrate high-performance nanowire transistors into logical inverters and fast ring oscillators on glass substrates. Applications include low-cost RFIDs and high-refresh-rate displays.

The idea is to assemble multi-nanowire transistors from solution on pieces of glass and plastic. The authors in [2] integrated two nanowire thin-film transistors to generate inverters (Fig. 2a). The results indicate fully interconnected nanowire oscillators could operate in the megahertz regime. The devices showed a maximum oscillation frequency of 11.7 MHz (Fig. 2d), corresponding to a stage delay of 14 ns. Nanowire oscillators made on glass substrates have higher frequencies than devices made on silicon substrates. This could be very beneficial for nanowire circuits since properties of devices made with other materials often degrade upon transfer to non-crystalline

substrates.

The techniques described in [2] are all compatible with low-deformation-temperature materials, most importantly plastics. One important limitation is that supply voltages of 35 V or more are required to achieve stable oscillations. However, the incorporation of high-k dielectrics, more advanced nanowire materials and reduced channel lengths could help improve the devices that use glass substrates. Advanced materials integration would enable these devices to be operated at lower voltages and much higher frequencies.

Can we make high performance logic gates using nanowires?

The authors in [3] suggest a “bottom-up” approach to building electronics from well-defined semiconductor nanowire building blocks. Crossed nanowire p-n junctions and junction arrays can be assembled to create integrated nanoscale FET arrays which can be configured as OR, AND, and NOR logic-gate structures. These structures exhibit substantial gain and have been used to implement basic computation.

CNTs are unsuited for the task because of our inability to control whether they are semiconducting or metallic. This makes device fabrication an arduous task. Nanowires, on the other hand, can be assembled in a predictable manner because the electronic properties and sizes of the nanowires can be precisely controlled during fabrication.

The authors in [3] synthesized single-crystal p-Si and n-GaN (gallium nitride) nanowires of diameters ranging from 10-30 nm. These nanowires were chosen because the oxide coating on their surfaces could be independently varied to enable good control of junction electronic properties. Both nanoscale diodes with low turn-on voltages as well as nanoscale FETs with high turn-on voltages can be made. In a typical NWFET, where the n-GaN nanowire is used as a nano-gate, we find a large decrease in conductance with increasing gate voltage. Crossed NWFETs are seen to be highly sensitive owing to their intrinsically thin gate dielectric between the crossed nanowires.

The bottom-up approach was used to investigate both diode- and FET-based logic gates (Fig. 6). First, a two-input OR gate was created by using a 2(p) by 1(n) cross p-n junction array with the two p-Si nanowires as inputs and the n-GaN nanowire as the output. The authors also fabricated an AND gate from a 1 (p-Si) by 3 (n-GaN) multiple junction array. In this structure, the p-Si nanowire is biased at 5 V; two of the GaN nanowires are used as inputs, and the third is used as a gate with a constant voltage to create a resistor by depleting a portion of the p-Si nanowire. Finally, a logic NOR gate was assembled by using a 1 (p-Si) by 3 (n-GaN) crossed NW-FET array. The NOR gate was configured with 2.5 V applied to one crossed nanowire FET to create a constant resistance of 100 MΩ, and the p-Si nanowire channel was biased at 5 V.

The two-input NOR gates routinely exhibited gains in excess of five. High gain is a critical characteristic of gates because it enables interconnection of arrays of logic gates without signal loss at

each stage. The authors also note that a multiple-input NOR gate can function as a NOT gate as well by eliminating one of the inputs.

Lastly, the authors interconnected multiple AND and NOR gates to implement basic computation in the form of an XOR gate, which corresponds to the binary logic SUM function. The XOR gate is configured by using the output from AND and NOR gates as the input to a second NOR gate (Fig. 4).

The authors in [3] note that further improvements can be made by assembling nanowires directly onto predefined metal electrode arrays and by creating more highly integrated circuit elements by feeding the output from one nanowire to the next.

What is the underlying physics behind nanostructures?

The performance of CMOS is expected to be enhanced by new physical phenomena. This includes quantum effects and ballistic transport in nanoscale devices. Bottom-up-type nanodevices formed by self-assembly are expected to become more prevalent. New types of nanoscale devices such as spin transistors will be integrated. The hope is that new physics that is observed on the nanoscale can be exploited to enhance the performance of CMOS beyond its scaling limit. Taking advantage of the quantum confinement effect can help us control and improve the performance of CMOS. The carriers within nanoscale narrow- and thin-channel MOSFETs can be confined into a one-dimensional narrow and thin channel respectively. More evidence of quantum effects is observed when the channel length is less than 10 nm. Further, the threshold voltage of narrow MOSFETs can be varied and controlled depending on the channel width because the ground energy of carriers is raised by quantum confinement.

Most importantly, the authors of [4] have demonstrated by simulation that the mobility is modified in narrow-channel MOSFETs. Larger mobility is observed in [100]-oriented devices: this is due to the anisotropic effective mass of silicon. Confinement in nanoscale narrow channels is stronger because the carriers have only one degree of freedom. The stronger the confinement, the greater the mobility. We also find that the thinner the silicon substrate, the lower the mobility due to increased acoustic phonon scattering. But p-MOSFETs have good mobility even with small thickness because the predominant scattering mechanism is scattering induced by silicon-on-insulator (SOI) thickness fluctuation. However, p-MOSFETs are less sensitive to SOI-thickness-fluctuation-induced scattering due to heavier hole effective mass normal to the channel surface. Thus in nanoscale CMOS, the crystal orientation, channel direction, and device dimension should be carefully determined in order to maximize device performance.

How can we exploit nanostructure physics for applications?

Note to TA: The following section is not an expected deliverable but exists solely for completeness. It is therefore not expected to count towards the 5-page limit.

The authors in [4] have a demonstrated a new function in silicon nanocrystal memories: silicon nanocrystals embedded in gate oxide act as site for charge storages. Physical separation of nanocrystals can improve the retention time by limiting lateral flow of charges.

A single-electron transistor is one of the best known nanoscale devices. A single-electron transistor, in the form of a point-contact MOSFET is made from a silicon quantum dot that is self-formed in the very narrow channel. Unfortunately, single-electron transistors generally operate only at very low temperatures. The operation temperature may be raised by making the quantum dot smaller. Currently, the dot size is 2 nm. Since the dot is extremely small, the quantum-level spacing in the dot is not negligible, and negative differential conductance (NDC) due to resonant tunneling is observed at room temperature. At room temperature, two integrated single-hole transistors exhibit Coulomb blockade oscillations and form a directional current switch. Moreover, each single-hole transistor has silicon nanocrystals embedded in the gate oxide which act as nonvolatile memory.

Further applications of single-electron/hole transistors are in digital circuit applications in the form of an XOR circuit, and an analog circuit application in the form of an analog pattern matching circuit since the Coulomb blockade oscillations have bell-shaped I-V characteristics.

References

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Ge/Si nanowire heterostructures as high-performance field-effect transistors

Jie Xiang[1]*, Wei Lu[1]*, Yongjie Hu[1], Yue Wu[1], Hao Yan[1] & Charles M. Lieber[1,2]

Semiconducting carbon nanotubes[1,2] and nanowires[3] are potential alternatives to planar metal-oxide-semiconductor field-effect transistors (MOSFETs)[4] owing, for example, to their unique electronic structure and reduced carrier scattering caused by one-dimensional quantum confinement effects[1,5]. Studies have demonstrated long carrier mean free paths at room temperature in both carbon nanotubes[1,6] and Ge/Si core/shell nanowires[7]. In the case of carbon nanotube FETs, devices have been fabricated that work close to the ballistic limit[8]. Applications of high-performance carbon nanotube FETs have been hindered, however, by difficulties in producing uniform semiconducting nanotubes, a factor not limiting nanowires, which have been prepared with reproducible electronic properties in high yield as required for large-scale integrated systems[3,9,10]. Yet whether nanowire field-effect transistors (NWFETs) can indeed outperform their planar counterparts is still unclear[4]. Here we report studies on Ge/Si core/shell nanowire heterostructures configured as FETs using high-κ dielectrics in a top-gate geometry. The clean one-dimensional hole-gas in the Ge/Si nanowire heterostructures[7] and enhanced gate coupling with high-κ dielectrics give high-performance FETs values of the scaled transconductance (3.3 mS μm^{-1}) and on-current (2.1 mA μm^{-1}) that are three to four times greater than state-of-the-art MOSFETs and are the highest obtained on NWFETs. Furthermore, comparison of the intrinsic switching delay, $\tau = CV/I$, which represents a key metric for device applications[4,11], shows that the performance of Ge/Si NWFETs is comparable to similar length carbon nanotube FETs and substantially exceeds the length-dependent scaling of planar silicon MOSFETs.

Silicon[9,10,12] and germanium[13,14] nanowires have been the focus of recent studies of one-dimensional (1D) FETs. However, metal contacts to single-component nanowires generally produce Schottky barriers that limit device performance[15], and moreover, scattering from charged dopants can also reduce the intrinsic mobility of these nanowire devices[15]. In contrast, we have recently demonstrated transparent contacts and low-bias ballistic transport[7] in undoped Ge/Si core/shell nanowire heterostructures (Fig. 1a, b), with an estimated scattering mean free path of ~500 nm. The 1D sub-band spacing in the typical 15-nm core Ge/Si nanowires determined through both experimental measurements and theoretical calculations[7] is ~25 meV, and thus at room temperature several sub-bands may participate in NWFET transport. While the Ge/Si nanowire devices will not be strictly 1D, the limited number of conduction channels and clean material structure can benefit performance through, for example, a reduction in scattering. To explore the potential of Ge/Si nanowire heterostructures as high-performance FETs we have fabricated (see Methods) devices using thin HfO_2 or ZrO_2 high-κ gate dielectrics and metal top gate electrodes (Fig. 1c, d). Cross-sectional transmission electron microscopy (TEM) images (Fig. 1e) show that both the high-κ and metal top gate conform to the approximately circular cross-section of the nanowire, and also verify the Ge/Si core/shell structure. The conformal top gate structure approaches an ideal cylindrical gate geometry, and together with the high-κ dielectrics produces a much more efficient gate response than previous studies using lower-κ SiO_2 dielectric and planar back gates[9,12,16].

Typical output and transfer characteristics recorded from a Ge/Si device fabricated in this way with a channel length, $L = 1$ μm and a total diameter of 18 nm (device A) are shown in Fig. 2a, b. The family of I_d–V_{ds} curves (Fig. 2a) show that the drain current I_d first increases then saturates with increasingly negative drain voltage, similar to a conventional long channel MOSFET[11]. These data also show that I_d increases as the gate voltage V_g decreases from 1 to −2 V, and thus that the device is a *p*-type depletion-mode FET. This *p*-type FET behaviour is expected from the band diagram in Fig. 1b, where the Fermi level lies below the Ge valence band edge in the absence of a gate. The I_d–V_g transfer curve recorded for the drain bias voltage

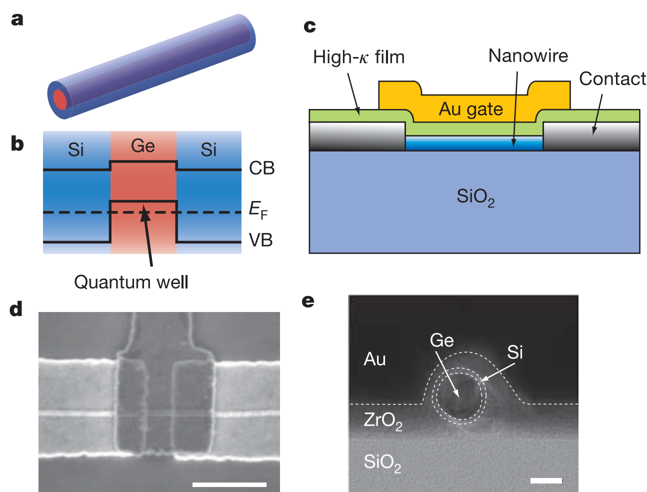

Figure 1 | Ge/Si core/shell NWFET. a, Schematic of a Ge/Si core/shell nanowire. **b**, Cross-sectional diagram showing the formation of hole-gas in the Ge quantum well confined by the epitaxial Si shell, where CB is the conduction band and VB is the valence band. The dashed line indicates the Fermi level, E_F. The valence band offset of ~500 meV between Ge and Si serves as a confinement potential to the hole-gas as discussed previously[7]. **c**, Schematic of the NWFET device with high-κ dielectric layer and Au top gate. **d**, Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar, 500 nm. **e**, Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Dotted lines are guides to the eye showing boundaries between different materials denoted in the image. The nanowire is tilted off the imaging axis. Scale bar, 10 nm.

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$V_{ds} = -1$ V (Fig. 2b) demonstrates that the NWFET has a peak transconductance, $g_m = dI_d/dV_g$, of 26 μS. In addition, the device exhibits a maximum drain current $I_{d(max)}$ of 35 μA at $V_g = -2$ V. We note these values of g_m and $I_{d(max)}$ substantially exceed the best performance reported to date in single semiconductor NWFETs[12,14].

The on current I_{on} for a FET device is usually determined at $V_g = V_{ds} = V_{dd}$, where V_{dd} is the power supply voltage and equals 1 V in our case. Following conventions in planar devices, we define on and off currents as the values measured at $V_{g(on)} = V_T - 0.7V_{dd}$ and $V_{g(off)} = V_T + 0.3V_{dd}$, so that 30% of the V_g swing above the threshold voltage V_T is applied to turn the device off, while the remaining 70% sets the operation range of the on state (Fig. 2b). Similar methods have been proposed in benchmarking carbon nanotube FET devices[4,17]. From Fig. 2b, we obtain $I_{on} = 14$ μA for this 1-μm-long device. Significantly, the scaled values of g_m and I_{on}, 1.4 mS μm^{-1} and 0.78 mA μm^{-1}, using the total nanowire diameter as the device width, already exceeds the values of 0.8 mS μm^{-1} and 0.71 mA μm^{-1} recently reported in much shorter, sub-100-nm silicon *p*-MOSFETs employing high-κ dielectrics[18].

In addition, we have prepared and studied a large number of Ge/Si NWFET devices with L varying from 1 μm to 190 nm; essentially all of these devices exhibited high-performance behaviour and testify to the reproducibility of both the Ge/Si nanowires and contacts to this material. Representative data obtained from a $L = 190$ nm device (device B), which should exhibit larger g_m and I_d values owing to reduced channel resistance, are shown in Fig. 2c. These data yield $g_m = 60$ μS, $I_{on} = 37$ μA ($V_{dd} = 1$ V), and $I_{d(max)} = 91$ μA, and correspond to scaled values of g_m and I_{on} of 3.3 mS μm^{-1} and 2.1 mA μm^{-1}, respectively. Notably, these values are more than twice that achieved in the longer channel device and are 3–4 times greater than state-of-the-art Si *p*-MOSFETs[18]. The geometric gate capacitance per unit area in our NWFETs, 44 fF μm^{-2} (Methods), is only 29% larger than the 34 fF μm^{-2} in these Si *p*-MOSFETs[18]. Therefore the large gain in g_m and I_{on} cannot be accounted for by an increase in gate capacitance alone. Moreover, the hole mobility for this Ge/Si NWFET, 730 cm^2 V^{-1} s^{-1}, extracted at the linear region ($|V_{ds}| = 10$ mV) from the peak $g_m = 3$ μS at $|V_g - V_T| = 0.13$ V using the charge control model, represents an improvement of more than a factor of ten over that of the Si *p*-MOSFET with HfO_2 gate dielectric (50–60 cm^2 V^{-1} s^{-1})[18], and also is more than twice the reported low-field mobility of Ge and strained SiGe heterostructure PMOS devices[19,20]. Improved mobility is observed for NWFETs with channel lengths from 0.19 to 1 μm (Supplementary Fig. S1), with an average of 640 cm^2 V^{-1} s^{-1}. These improvements over planar device structures thus verify the performance benefit due to the quasi-1D transport in clean Ge/Si heterostructure nanowires.

The subthreshold region of the I_d–V_g data was also analysed and yields values of the slope, $S = -[d(\log_{10} I_d)/dV_g]^{-1}$, of 105 and 100 mV per decade for the $L = 1$ μm and 190 nm NWFETs, respectively, for $V_{ds} = -1$ V (Fig. 2b, c). Similar values of S were obtained from I_d–V_g data recorded on both devices using V_{ds} from −0.01 to −1 V, which indicate the absence of significant short-channel effects[11] for devices down to at least $L = 190$ nm and excellent V_g control of the channel potential over the competing effect of drain-induced barrier lowering at larger biases[11].

In general, an FET with a small S is essential for modern logic circuits as it reduces the off state current and minimizes static power dissipation. The value of S can be estimated[11] by $2.3k_BT/e\alpha$, where T is temperature and α is the gate-coupling factor, which yields a room temperature minimum ($\alpha = 1$) of 60 mV per decade. The values of S determined for the $L = 1$ μm and 190 nm Ge/Si NWFETs are superior to the best value (140 mV per decade) reported previously[9] for NWFETs but still larger than the theoretical minimum. The non-ideal gate coupling ($\alpha < 1$), which yields this larger S value, is probably due to a finite trap state density at the nanowire/high-κ interface[21]. Optimization of the high-κ deposition process during fabrication or growth of a cylindrical high-κ shell on the Ge/Si nanowire before fabrication should yield improved interface quality and enable us to approach ideal subthreshold behaviour in the future in these NWFETs.

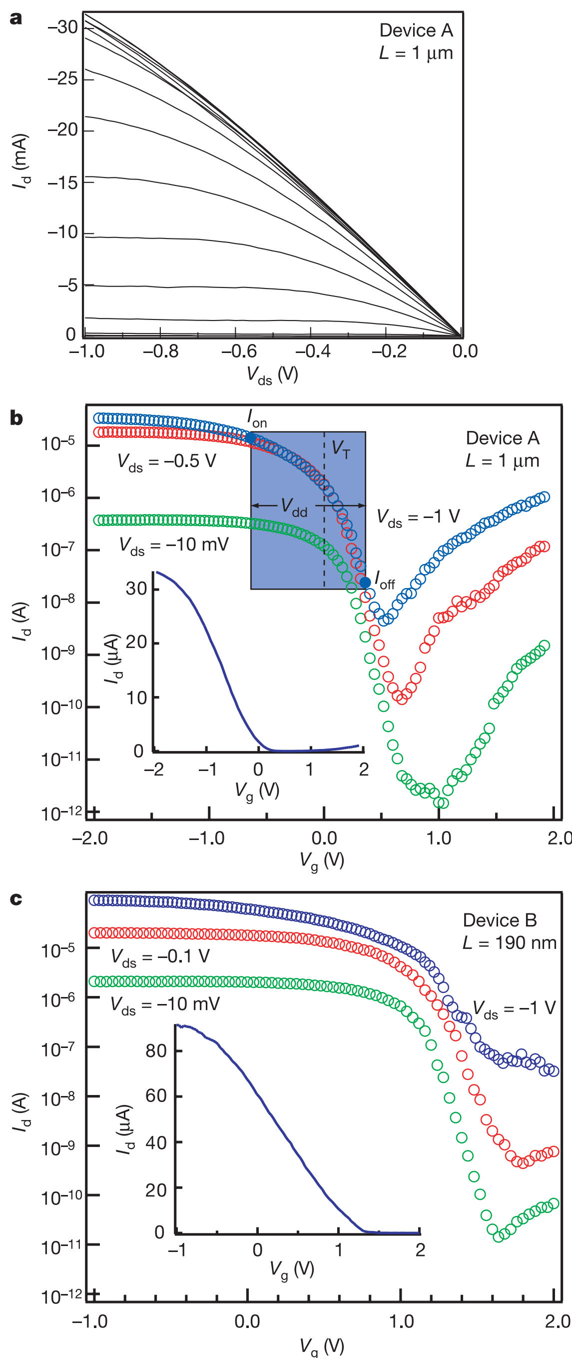

Figure 2 | Characteristics of high-performance Ge/Si NWFET. a, I_d–V_{ds} data for device A ($L = 1$ μm, 4 nm HfO_2 dielectric) with $V_g = -2$ to 2 V in 0.25 V steps from top to bottom. **b,** I_d–V_g for device A with blue, red, and green data points corresponding to V_{ds} values of −1, −0.5 and −0.01 V, respectively. The leakage current through the gate electrode (I_g) is $<10^{-10}$ A, which excludes I_g as source of increase in I_d at $V_g > \sim 0.5$ V. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V. The blue-shaded area defines the 1 V gate voltage window described in the text, where V_T was determined from the intercept of the tangent of maximum slope (linear transconductance) region of the I_d–V_g curve[11]. **c,** I_d–V_g data for device B ($L = 190$ nm, 4 nm HfO_2 dielectric) with blue, red and green data points corresponding to V_{ds} values of −1, −0.1 and −0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V.

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An important benchmark of transistor performance is the intrinsic delay, $\tau = CV/I$, where C is the gate capacitance, $V = V_{dd}$, and I is on current I_{on}. As defined, τ represents the fundamental RC (where R is the device resistance and C is the capacitance) delay of the device and provides a frequency limit for transistor operation that is relatively insensitive to gate dielectrics and device width, and thus represents a good parameter for comparing different types of devices[11]. The calculated intrinsic delays are 57 and 4 ps for devices A and B in Fig. 2, respectively, where C was determined by numerical simulation (Methods). A summary of the results from seven Ge/Si NWFETs versus L and the corresponding scaling for Si MOSFETs (Fig. 3a) highlights several key points. First, the data show clear speed advantage at a given L for the Ge/Si NWFETs versus Si p-MOSFETs. For example, the intrinsic delay for a 190 nm Si planar device is larger than 10 ps, about three times longer than our device B. Second, the delay time for the 190 nm Ge/Si device is about the same as that of similar-length CNTFET devices[4]. Last, length scaling of τ is more favourable for our Ge/Si NWFETs than Si MOSFETs (that is, slope of $\sim$1.5 versus $\sim$1.1). We attribute this important difference to a suppression of scattering in the quasi-1D quantum confined Ge/Si nanowires versus MOSFETs[22], although additional studies will be needed to support this idea.

To capture the off state leakage current property, we used a method described by ref. 17 and studied the CV/I_{on} versus I_{on}/I_{off} ratio. Here we assume full control of the threshold voltage, allowing a window of $V_{g(on)}–V_{g(off)} = V_{dd} = 1$ V to move along the V_g axis and define a pair of I_{on} and I_{off} value from the $I_d–V_g$ data plot. The CV/I_{on} versus I_{on}/I_{off} data for devices A and B (Fig. 3b) shows the trade-off between high speed and small leakage. The smallest τ is observed at the largest I_{on}, although this corresponds to a minimum on/off ratio. As the on/off ratio increases τ also increases[4], until the on/off ratio reaches a maximum limited by ambipolar conduction (see below). The arrows correspond to the intrinsic delay values obtained from the 70–30% criteria used to define I_{on} in the benchmark plot in Fig. 3a, and show that the I_{on}/I_{off} ratios for the A and B devices are 100 and 580, respectively. On/off ratios for the rest of the devices in Fig. 3a all lie within this range. The on/off ratio is expected to reach $10^4–10^5$ as the subthreshold slope is improved to the ideal value of 60 mV per decade. Studies of strained SiGe planar devices show that subthreshold slopes of 66–70 mV per decade are achievable[20], although we note that the on/off ratio of 10^2 may already meet a lower practical limit for certain high-performance applications[23].

The above Ge/Si NWFETs are depletion-mode devices with threshold voltages $V_T > 0$, and require $V_g > V_T$ to be turned off. However, enhancement-mode FETs with $V_T < 0$, which are off for $V_g = 0$, are technologically more desirable because they consume less static power. In addition and as discussed above, obtaining the optimal device operation depends critically on the full control of the threshold voltage. We have exploited the top gated structure (Fig. 1c) to tune V_T through variations in the gate metal work function. Comparison of $I_d–V_g$ data recorded using Au and Al metal gates (Fig. 4a) clearly shows a change from depletion mode, $V_T = +0.65$ V, to enhancement mode $V_T = -0.65$ V, while other key device parameters remain the same. Measurements made on 68 NWFETs yield average threshold values of 0.53 ± 0.17 and

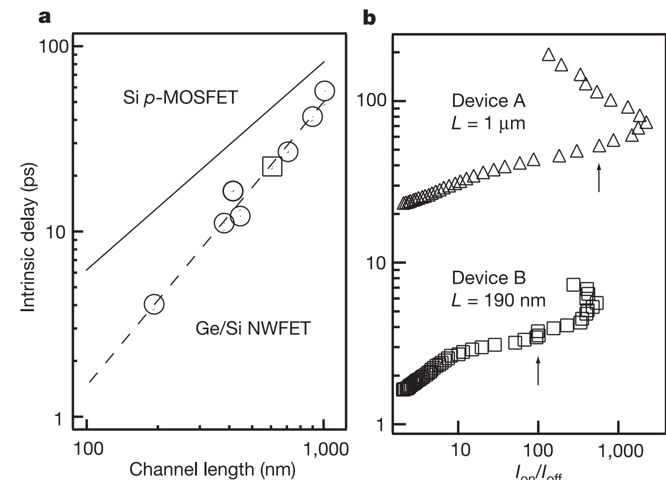

Figure 3 | Benchmark and comparison of Ge/Si FETs. **a**, Intrinsic delay τ versus channel length for seven different Ge/Si nanowire devices with HfO_2 dielectric (open circle) and ZrO_2 dielectric (open square). Data for devices A and B are included. The I_{on} values were measured at $V_{g(on)} = V_T - 0.7V_{dd}$, as discussed in the text. The dashed line is a fit to the data points while solid line is the Si p-MOSFET results from ref. 4. **b**, Intrinsic delay versus on/off ratio for the two devices in Fig. 2. Arrows indicate the values of intrinsic delay used in **a**.

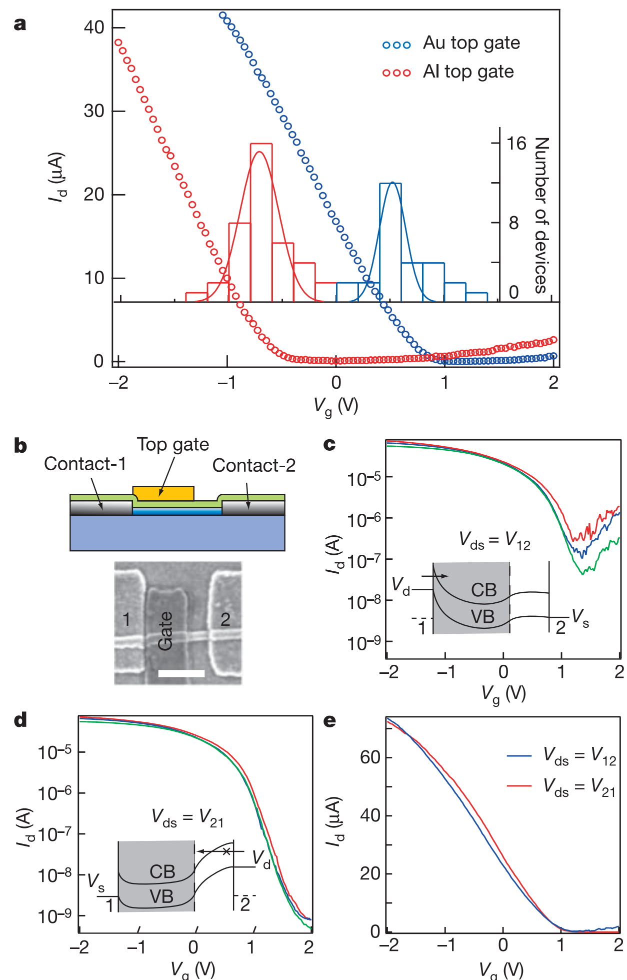

Figure 4 | Control of threshold voltage and ambipolar conduction through device design. **a**, $I_d–V_g$ curves for two $L = 300$ nm devices with Au (blue) and Al (red) top gate electrodes ($V_{ds} = -1$ V). Inset shows histogram of V_T with the same V_g axis for a total of 68 $L = 300$ nm devices with Au (blue) and Al (red) top gates. Solid lines correspond to gaussian fits to the two distributions. **b**, Schematic and SEM image of the asymmetrical gate structure designed to suppress ambipolar conduction. Scale bar, 300 nm. **c**, $I_d–V_g$ of partially gated device with ambipolar conduction; bias was applied to contact 1 ($V_{ds} = V_{12}$). Inset, schematic of band bending in the NWFET at finite bias. Arrow denotes electron injection at the drain contact. **d**, $I_d–V_g$ for $V_{ds} = V_{21}$. Inset, schematic of band bending with electron injection denoted by arrow. The red, blue and green curves in **c** and **d** correspond to V_{ds} values of −1, −0.8 and −0.6 V, respectively. **e**, Linear scale $I_d–V_g$ ($V_{ds} = -1$ V) for the devices in **c** and **d**. The two devices have the same peak $g_m = 35$ μS and $I_{d(max)} = 73$ μA.

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-0.72 ± 0.25 V for Au and Al top gates, respectively, and thus demonstrate the reproducibility of this effect in our high-performance Ge/Si NWFETs. The V_T shift of 1.25 V corresponds approximately to the work function difference between Au ($\Phi_{Au} = 5.31$–5.47 eV) and Al ($\Phi_{Al} = 4.28$ eV) with small deviations attributable to metal/dielectric interface states[24]. More generally, these results indicate that it will be possible to tune V_T for specific applications simply through a choice of top gate metal with specific work function in fabrication.

The Ge/Si NWFETs also exhibit an increase in I_d when V_g is increased to larger positive values (for example, Fig. 2) owing to conduction by electron carriers (versus holes). Similar ambipolar conduction has been observed in high-performance CNTFETs with metal contacts[4,25,26], and is deleterious for applications since it reduces the window of operation and increases the minimum off-state current. To address this issue we characterized devices with asymmetrical partial gates (Fig. 4b). Data recorded from a NWFET with bias voltage applied to contact 1 (proximal to the gate) and holding contact 2 at ground (Fig. 4c), $V_{ds} = V_{12}$, show ambipolar conduction like the fully gated device in Fig. 2. Significantly, switching the source and drain electrodes ($V_{ds} = V_{21}$) dramatically suppresses the ambipolar current from 300 to 0.8 nA at $V_{ds} = -1$ V (Fig. 4d). These results can be explained by the corresponding band diagrams (insets, Fig. 4c, d). In the first case, electron injection at the drain increases with increasing V_g and ultimately dominates the current, while in the second, the ungated region near contact 2 acts as a thick barrier to electron transport and suppresses electron current even at large downward bending of the conduction band.

Importantly, the reduction in ambipolar current using this device structure does not limit other key NWFET characteristics. The on state conductance and transconductance (Fig. 4e) show no degradation compared to fully gated devices with similar dimensions (for example, Fig. 4a), and S (Fig. 4d) shows little V_{ds} dependence, indicating excellent gate control[11]. These observations contrast with experiments on CNTFETs with similar gate structures[27], which may have been limited by the presence of Schottky barriers at the CNT contacts. Such limitations do not exist for Ge/Si NWFETs, which do not have contact barriers[7], and thus the asymmetrical gate structure can yield unipolar NWFETs without sacrificing performance.

In summary, we have demonstrated top-gated Ge/Si NWFET heterostructures with high-κ dielectrics that exhibit scaled transconductance and on-current values of 3.3 mS μm^{-1} and 2.1 mA μm^{-1}, respectively, which are three to four times greater than those for state-of-the-art MOSFETs. In addition, the Ge/Si NWFET hole mobility, 730 $cm^2 V^{-1} s^{-1}$, is more than a factor of ten greater than the Si p-MOSFET with HfO_2 gate dielectric[18] and more than twice that of Ge and strained SiGe heterostructure PMOS devices[19,20]. These values, together with the demonstrated control over threshold voltage and ambipolar behaviour, suggest substantial promise of Ge/Si NWFETs, although further performance improvements at the single device level should also be possible through optimization of gate coupling and size scaling[28]. Looking to the future, the ability to prepare high-performance Ge/Si NWFETs in close to 100% yield, which represents a distinct advantage over similar performance CNTs, and assemble nanowires *en masse* in addressable arrays[9] could open up advances and applications in several areas, including high-frequency electronics on plastic and glass substrates[10], higher-sensitivity nanosensors[29], and possibly extending the roadmap for high-performance logic.

METHODS

Fabrication and measurement of Ge/Si NWFET devices. The growth of epitaxial core/shell Ge/Si nanowires and fabrication of Ni-contacted NWFETs are described elsewhere[7]. Nanowires have an average core diameter of 14.6 nm and Si shell thickness of 1.7 nm, and normally exhibit <110> growth direction. A thin high-κ dielectric film was deposited on the devices using the atomic layer deposition (ALD) process. 30 cycles for HfO_2 deposition and 50 cycles for ZrO_2 were used at 110 °C with each cycle consisting of 1 s water vapour pulse, 5 s N_2 purge, 3 s precursor, and 5 s N_2 purge. Tetrakis(dimethylamino) hafnium [$Hf(N(CH_3)_2)_4$], and tetrakis(dimethylamino) zirconium were used as precursors. Electron beam lithography was used to define the top gate, followed by thermal evaporation of either Cr/Au (5 nm/50 nm) or Al (50 nm). The devices were measured at room temperature in vacuum ($P < 10^{-4}$ torr) with a probe station (TTP-4, Desert Cryogenics).

Cross-sectional TEM sample preparation. Dry-transfer from the growth substrate was used to deposit aligned nanowire arrays with inter-nanowire spacings of several micrometres on a Si/SiO_2 wafer. The wafer was then coated with a thin film of ZrO_2 high-κ dielectric and Au metal as described above. Cross-sectional TEM samples were prepared by cutting the wafer into thin slices, followed by mechanical polishing and further thinning by ion milling. TEM images were taken by a JEOL 2010F high-resolution microscope.

Calculation of mobility and intrinsic delay *CV/I*. The gate capacitance, C, was calculated using numerical simulations on nanowire devices with a Ge core diameter of 14.6 nm and a Si shell thickness of 1.7 nm; these parameters were determined for devices using cross-sectional TEM measurements. The thickness for HfO_2 ($\kappa = 23$) and ZrO_2 ($\kappa = 20$) are 4 and 7 nm, respectively. Assuming the top gate conformally covers the top half of the nanowire as indicated by the cross-sectional TEM image, we obtained the gate capacitances per unit length of $C_L = 800$ aF μm^{-1} (HfO_2) and 580 aF μm^{-1} (ZrO_2) from two-dimensional electrostatic simulations (Quickfield, Tera Analysis, Denmark). When scaled using the total diameter of the nanowire, we obtained gate capacitances per unit area of 44 and 32 fF μm^{-2} for the HfO_2 and ZrO_2 dielectrics used, respectively. We note that the calculation tends to overestimate the gate coupling capacitance because it does not include the effect of quantum capacitance from the finite density of states in the 1D Ge channel[30], and does not consider the formation of interfacial silicon oxide layer that tends to reduce the κ value. Mobility is calculated from low-bias g_m based on the charge control model: $\mu = \frac{g_m}{V_{ds}} \cdot \frac{L^2}{C}$, where L is device gate length. Supplementary Fig. S1 shows a linear relationship between the inverse transconductance and the channel length for three different devices, consistent with this model. For the intrinsic delay CV/I_{on}, $V = V_{dd} = 1$ V is the power supply voltage for both the V_g swing and saturation bias.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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High-speed integrated nanowire circuits

Inexpensive sophisticated circuitry can be 'painted' on to plastic or glass substrates.

Macroelectronic circuits made on substrates of glass or plastic could one day make computing devices ubiquitous owing to their light weight, flexibility and low cost[1]. But these substrates deform at high temperatures so, until now, only semiconductors such as organics and amorphous silicon[2] could be used, leading to poor performance. Here we present the use of low-temperature processes to integrate high-performance multi-nanowire transistors into logical inverters and fast ring oscillators on glass substrates. As well as potentially enabling powerful electronics to permeate all aspects of modern life, this advance could find application in devices such as low-cost radio-frequency tags and fully integrated high-refresh-rate displays.

The mobility of single-crystal semiconducting nanowires is comparable to that of computer-grade silicon[3]. Multi-nanowire transistors[4,5] — analogous to thin-film transistors — can be assembled from solution on pieces of glass and plastic[6]. For many applications, however, fully interconnected nanowire devices that function as viable circuit elements operating at high frequencies will be required.

We integrated two nanowire thin-film transistors to generate inverters (Fig. 1a), which we made in a parallel process over glass substrates by using standard photolithography techniques (for methods, see supplementary information). The process gives a high yield of devices that show reliable, well defined signal inversion under direct current conditions (see supplementary information). Investigation of the alternating-current response of these inverters (Fig. 1b) shows that the gain, or signal amplification, is greater than unity, and the expected phase inversion is achieved when these devices are driven by a 1-MHz sine wave at a supply of 15 V. As signal propagation in an integrated system requires gain that is greater than unity, these results and the high reproducibility of our nanowire transistors suggest that fully interconnected nanowire oscillators could operate in the megahertz regime.

Our ring oscillators consist of three inverters in series (Fig. 1c), where the input of each inverter is connected to the output of the previous device, with a feedback loop to complete the ring. The necessary on-chip integration is achieved during fabrication and does not require any external wiring. We characterized the nanowire ring oscillators on glass substrates and found that the output-voltage oscillations were stable and self-sustained.

The devices show a maximal oscillation frequency of 11.7 MHz, corresponding to a stage delay of 14 ns (Fig. 1d). Significantly, all devices measured on glass have oscillation frequencies at or above 10 MHz. Furthermore, nanowire oscillators made on glass substrates have higher frequencies than devices made on silicon substrates (see supplementary information). This could be a key advantage for nanowire circuits as the properties of devices made with other materials often degrade upon transfer to non-crystalline substrates[7].

The stable oscillation frequencies seen for our nanowire-based devices are many orders of magnitude larger than previous ring oscillators based on nanoscale building blocks. For example, carbon-nanotube devices have oscillation frequencies from 5 to 220 Hz (refs 8, 9). Although this is not an intrinsic limit for nanotubes, it highlights how important reproducible material properties are for the successful creation of integrated, high-performance devices.

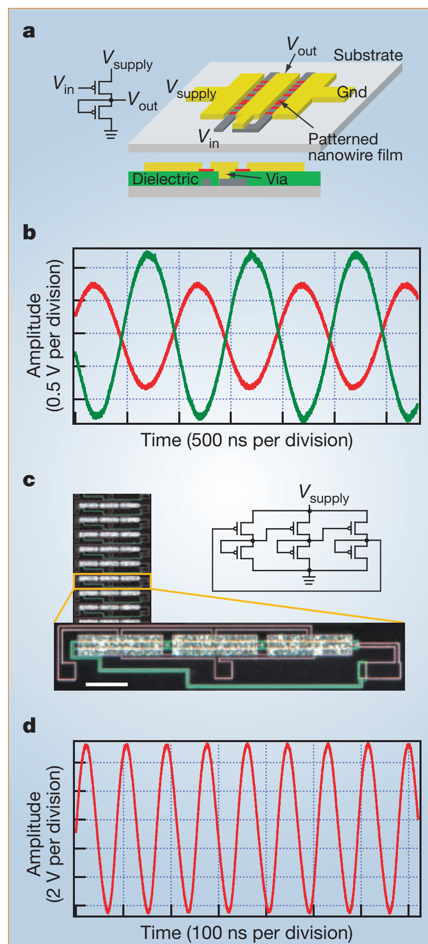

Figure 1 Alternating-current properties of integrated multi-nanowire circuits on glass. **a**, Circuit diagram and schematics of the multi-nanowire inverters. Labelled voltages are bias (V_{supply}), input (V_{in}) and output (V_{out}) voltage. The dielectric is omitted in the perspective schematic for clarity. 'Via' indicates one of a pattern of holes in the dielectric layer that are used to connect different metal layers. **b,** Output waveform (green) of an inverter fabricated on glass driven by a 1-MHz sine wave (red) with $V_{supply} = 15$ V. **c,** Optical images and circuit diagram of nanowire ring oscillators. The gate level edge, source-drain level edge and nanowires appear green, pink and white, respectively, in dark field. Scale bar, 100 µm. **d**, Oscillation of 11.7 MHz in a ring oscillator structure with $V_{supply} = 43$ V.

It is interesting to compare these nanowire-device features with those of organic ring oscillators, given that the active material in both can be deposited at ambient temperatures from liquid solutions. Reported stage-delay times for organic ring oscillators are typically longer than 300 ns (ref. 10) and therefore substantially (20×) slower than those we obtain for nanowires on glass. Comparable results have been seen for other semiconductors with low synthesis temperatures; to our knowledge, the fastest reported stage delay for amorphous silicon ring oscillators is 210 ns (ref. 11).

Our integrated nanowire-based transistors open the way to a variety of electronic applications; the techniques we describe are all compatible with low-deformation-temperature materials such as plastics, broadening the scope for design. One limitation is that supply voltages of 35 volts or more are required to achieve stable oscillations, but device structures could be improved by incorporating higher-*k* dielectrics, more advanced nanowire materials and reduced channel lengths. This would enable them to be operated at lower voltages and much higher frequencies, taking low-cost electronics to high-performance computing levels.

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Logic Gates and Computation from Assembled Nanowire Building Blocks

Yu Huang, *et al.*

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in untreated cells. For degradation assays, cells were incubated at 25°C for 1 hour, and receptor number (total specific ^{125}I-CYP binding sites) was determined after 24 hours of isoproterenol treatment and expressed as the percentage of receptor number assessed in nonstimulated cells. Where necessary, MG132 (20 μM) or lactacystin (20 μM) mixed in serum-free media was added to cells 1 hour before stimulation.
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27. A cDNA construct of β-arrestin2 was cloned into pET-29a and was used to isolate recombinant S·TAG-β-arrestin2His6 purified on S-protein agarose beads (Novagen), which was then used as the substrate in the β-arrestin2 in vitro ubiquitination reaction containing 20 mM Hepes (pH 7.5), 5 mM $MgCl_2$, 2 mM DTT, 2 mM ATP, 5 μg of ubiquitin, 20 μM MG132, and crude RRL, either supplemented or not with 100 μg of COS cell extract (clarified by centrifugation at 21,000*g* for 15 min) with or without overexpressed Mdm2.
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REPORTS

Logic Gates and Computation from Assembled Nanowire Building Blocks

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Miniaturization in electronics through improvements in established "top-down" fabrication techniques is approaching the point where fundamental issues are expected to limit the dramatic increases in computing seen over the past several decades. Here we report a "bottom-up" approach in which functional device elements and element arrays have been assembled from solution through the use of electronically well-defined semiconductor nanowire building blocks. We show that crossed nanowire p-n junctions and junction arrays can be assembled in over 95% yield with controllable electrical characteristics, and in addition, that these junctions can be used to create integrated nanoscale field-effect transistor arrays with nanowires as both the conducting channel and gate electrode. Nanowire junction arrays have been configured as key OR, AND, and NOR logic-gate structures with substantial gain and have been used to implement basic computation.

Fundamental physical constraints and economics are expected to limit continued miniaturization in electronics by conventional top-down manufacturing during the next one to two decades (*1*, *2*) and have thus motivated efforts world wide to search for new strategies to meet expected computing demands of the future. Bottom-up approaches to nanoelectronics (*2*), where the functional electronic structures are assembled from well-defined nanoscale building blocks, such as carbon nanotubes (*3–8*), molecules (*9–11*), and/or semiconductor nanowires (*12–14*), have the potential to go far beyond the limits of top-down manufacturing. For example, single-walled carbon nanotubes (NTs) have been used as building blocks to fabricate room-temperature field-effect transistors (FETs) (*3–5*), diodes (*6*, *7*) and recently, an inverter (*8*), which represents a key component for logic. However, the inability to control whether NTs are semiconducting or metallic (*2*, *5*) makes specific device fabrication largely a random event and poses a serious issue for integration beyond the single–device element level. A potential solution to the prob-

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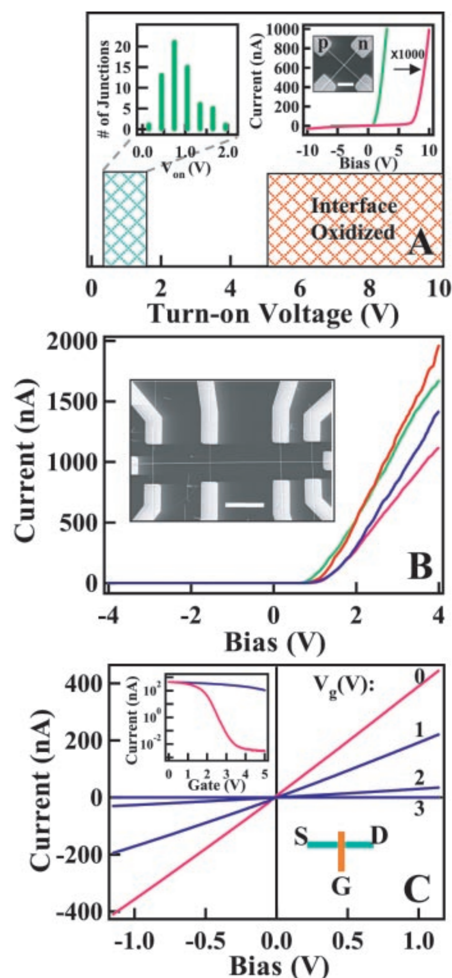

Fig. 1. Crossed NW nanodevice elements. (**A**) Turn-on voltage distribution for crossed NW junctions. The green cross-hatched area indicates the range for low turn-on voltage junctions formed from as-assembled NW junctions, and the red cross-hatched area indicates high turn-on voltage devices after local oxidation of the junction. (Top left inset) Histogram of turn-on voltage for over 70 as-assembled junctions showing a narrow distribution around 1 V. The high turn-on voltage devices have a broad distribution but generally fall into the range of 5 to 10 V. (Top right inset) An example of an *I-V* response for low (green) and high (red) turn-on voltage elements. The red curve is multiplied by 1000 for better viewing. The inset inside the top right inset shows a typical scanning electron micrograph (SEM) of a crossed NW device. Bar: 1 μm. (**B**) *I-V* behavior for a 4(p) by 1(n) multiple junction array. The four curves represent the *I-V* response for each of the four junctions and highlight reproducibility of assembled device elements. (Inset) An example of a multiple crossed NW device. Bar: 2 μm. (**C**) Gate-dependent *I-V* characteristics of a crossed NW-FET. The NW gate voltage for each *I-V* curve is indicated (0, 1, 2, and 3 V). (Top left inset) The red and blue curves show *I* versus V_{gate} for n-NW (red) and global back (blue) gates when the bias is set at 1 V. The transconductance for this device was 80 and 280 nS (V_{sd} = 1 V) when using the global back gate and NW gate, respectively. (Bottom right inset) The measurement configuration.

lem of coexisting metallic and semiconducting NTs involves selective destruction of metallic tubes (*5*), although such an approach requires extensive top-down lithography and subsequent processing to implement.

Semiconductor nanowires (NWs) have also been used as building blocks for assembling a range of nanodevices including FETs (*12*, *13*), p-n diodes (*13*, *14*), bipolar junction transistors, and complementary inverters (*14*). In contrast to NTs, these NW devices can be assembled in a predictable manner because the electronic properties and sizes of the NWs can be precisely controlled during synthesis (*12–15*) and methods exist for their parallel assembly (*16*). However, previous NW and NT single device elements represent only an initial step toward nanoelectronic systems, which will require both the formation of device elements and integrated device arrays in high yield. To this end, we report assembly of p-type silicon (p-Si) and n-type gallium nitride (n-GaN) NWs to form crossed nanoscale p-n junctions and junction arrays in which the electronic properties and function are controlled in a predictable manner to provide both diode and FET elements in high yield. Importantly, nanoscale p-n junction and FET arrays have been configured as OR, AND, and NOR logic gates with substantial gain, and these gates have been interconnected to demonstrate computation with a half-adder. Our approach leads naturally through the bottom-up paradigm to integration at the nanoscale and represents a step toward the creation of sophisticated nanoelectronics.

The single-crystal p-Si and n-GaN NWs used in this study were synthesized by nanocluster-catalyzed methods described previously (*14*, *15*, *17*, *18*) and had diameters of 10 to 25 and 10 to 30 nm, respectively, although NWs as small as 2 nm can be prepared (*15*). These NWs were chosen for our studies because the oxide coating on their surfaces can be independently varied (*18*) to enable good control of junction electronic properties. To demonstrate this feature, which is critical for assembly of more complex integrated devices, we have assembled and characterized the electronic properties of a large number of crossed p-Si/n-GaN junctions (*18*) (Fig. 1). Current-voltage (*I-V*) measurements show that the p-Si/n-GaN crossed NW devices exhibit current rectification characteristic of p-n diodes with a typical turn-on voltage of about 1.0 V (Fig. 1A) (*19*). These results are highly reproducible: Current rectification was observed in over 95% of the more than 70 crossed p-n NW devices studied, and in addition, 85% of the devices exhibited low turn-on voltages between 0.6 and 1.3 V (Fig. 1A, top left inset). The reproducible assembly of crossed NW structures with predictable electrical properties contrasts sharply with results from NT-based devices and has enabled us also to explore the assembly and properties of integrated p-n junction arrays. Importantly, electrical transport measurements made on a typical 4 by 1 crossed p-Si/n-GaN junction array (Fig. 1B) show that the four nanoscale cross points form independently addressable p-n junctions with clear current rectification and similar turn-on voltages. These data demonstrate the high yield and reproducibility of our crossed NW p-n devices and represent an important and necessary step for the rational assembly of more complex devices such as logic gates (see below).

In addition to these low turn-on voltage diodes, high turn-on voltage p-n junctions can be used as nanoscale FETs (Fig. 1C). Specifically, a p-channel FET with both a nanoscale conducting channel and a nanoscale gate is formed from a n-GaN/p-Si crossed NW structure; we refer to these structures as crossed NW FETs (cNW-FETs). The high turn-on voltage junctions required to assemble cNW-FETs were reproducibly formed by increasing the oxide layer thickness at the junctions by either thermal oxidation of the SiNWs (*18*) or by passing a high current through the junction in the air (*20*). Transport data recorded on over 50 p-n junctions prepared in this way (Fig. 1A) show that turn-on voltages greater than 5 V can be achieved in nearly quantitative yield, while still maintaining good conduction through individual NWs. The corresponding *I-V* data recorded on a typical cNW-FET, where the n-GaN NW is used as a nano-gate, exhibit a large decrease in conductance with increasing gate voltage (Fig. 1C) (*21*). Specifically, the conductance can be changed by a factor of more than 10^5 with only a 1- to 2-V variation in the nano-gate, whereas the conductance changes by only a factor of 10 when a global back-gate is used (Fig. 1C, top left inset). We attribute the high sensitivity of the cNW-FETs to the intrinsically thin gate dielectric between the crossed NWs, although a complete understanding of this new type of FET will require further investigation. The reproducibility, large gate response, and potential for nanoscale integration make the cNW-FETs attractive for assembling more complex electronic devices in which FETs are critical elements (*22*). In addition, these characteristics contrast recent work on NTs (*3–5*, *8*) that have used either global back gates, which are incompatible with independent device function, or lithographically defined local gates, which use and are constrained by conventional lithography to obtain nanoscale structures.

The high-yield assembly of crossed NW p-n junctions and cNW-FETs enables the bottom-up approach to be used for formation of more complex and functional electronic devices, such as logic gates. To demonstrate the flexibility of these NW device elements, we have investigated both diode- and FET-based

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logic (*23*). First, a two-input OR gate was realized by using a 2(p) by 1(n) crossed p-n junction array with the two p-Si NWs as inputs and the n-GaN NW as the output (Fig. 2A). In this device, the output is low (logic 0) when both input voltages are low (0 V), and the output is high (logic 1) when either or both of the input voltages are high (5 V) (Fig. 2B), where a high input corresponds to forward bias of the corresponding p-n junction. The output-input (V_o-V_i) voltage response (Fig. 2B, inset) shows that V_o increases linearly with V_i when one input is set low (0 V), except for the region near 0 V. This low-response region is due to the finite turn-on voltage of the p-n junctions and produces a logic output typically 0.4 to 0.2 V less than the input voltage. Small reductions in V_o do not affect the operation of our logic gates because the low turn-on voltage contributions are reproducible and can be readily accounted for in defining the 0 and 1 states. The V_o-V_i data also show a nearly constant high output when the second input is set high (5 V). The experimental truth table for the 1 by 2 crossed NW device (Fig. 1C) summarizes the input-output response and confirms that this NW device behaves as a logic OR gate. We also note that assembly of more p-n junctions would produce a multiple input OR gate, i.e., a 1 by *n* junction array for an *n*-input OR gate.

We have also fabricated an AND gate from a 1(p-Si) by 3(n-GaN) multiple junction array (Fig. 2D). In this structure, the p-Si NW is biased at 5 V; two of the GaN NWs are used as inputs, and the third is used a gate with a constant voltage to create a resistor by depleting a portion of the p-Si NW. The logic 0 is observed from this device when either one or both of the inputs are low (Fig. 2E), because $V_i = 0$ corresponds to a forward-biased, low-resistance p-n junction that pulls down the output (logic "0"). The logic 1 is observed only when both inputs are high, because this condition corresponds to reverse-biased p-n diodes with resistances much larger than that of the constant resistor, i.e., there is a small voltage drop across the constant resistor and a high voltage is achieved at the output. The V_o-V_i data (Fig. 2E, inset) shows constant low V_o when the other input is low and nearly linear behavior when the other input is set at high. The truth table for the NW device (Fig. 2F) summarizes the input-output response and confirms that this device functions as a logic AND gate.

In addition, a logic NOR gate was assembled by using a 1(p-Si) by 3(n-GaN) cNW-FET array (Fig. 2G). The NOR gate was configured with 2.5 V applied to one cNW-FET to create a constant resistance of ~100 megohms, and the p-SiNW channel was biased at 5 V. The two remaining n-GaN NW inputs act as gates for two cNW-FETs in series. In this way, the output depends on the resistance ratio of the two cNW-FETs and the constant resistor. The logic 0 is observed when either one or both of the inputs is high (Fig. 2H). In this case, the transistors are off and have resistances much higher than that of the constant resistor, and thus most of the voltage drops across the transistors. A logic 1 state can only be achieved when both of the transistors are on, i.e., when both inputs are low. The V_o-V_i relation (Fig. 2H, inset) shows constant low V_o when the other input is high, and a nonlinear response with large change in V_o when the other input is set low. Analysis of these data and those from similar structures demonstrates that these two-input NOR gates routinely exhibit gains in excess of five, which is substantially larger than the gain reported for complementary inverters based on Si-NWs (*14*) and carbon NTs (*8*). High gain is a critical characteristic of gates because it enables interconnection of arrays of logic gates without signal restoration at each stage (*24*). The truth table for this NW device (Fig. 2I) summarizes the V_o-V_i response and demonstrates that the device behaves as a logic NOR gate. Lastly, our multiple-input logic NOR gates can function as NOT gates (simple inverters) by eliminating one of the inputs.

The predictable assembly of logic OR, AND, and NOR (NOT) gates enables the organization of virtually any logic circuit and represents a substantial advance compared with previous studies of NTs and molecular systems. First, the controllable electronic characteristics of the NW building blocks and reproducible properties of the devices assembled from these blocks contrast with the much lower control achieved to date with NTs (*3–8*). We believe that predictable and reproducible assembly of device elements

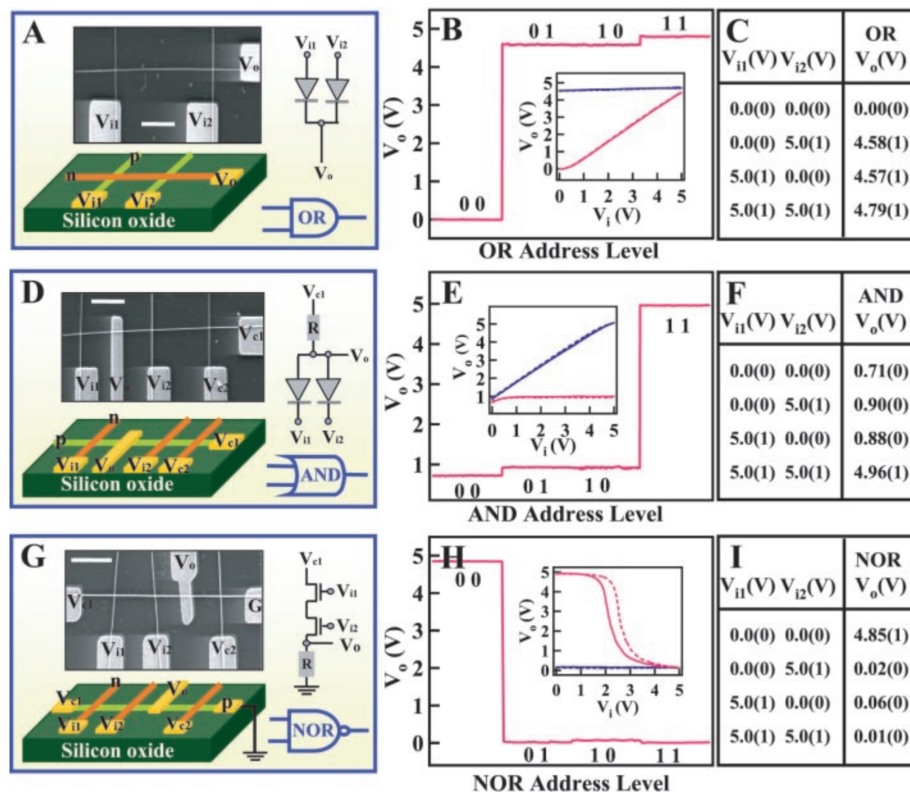

Fig. 2. Nanowire nano-logic gates. (**A**) Schematics of logic OR gate constructed from a 2 by 1 crossed NW p-n junction. (Insets) An example SEM (bar: 1 μm) of the assembled "OR" gate and symbolic electronic circuit. (**B**) The output voltage versus the four possible logic address level inputs: (0,0); (0,1); (1,0); (1,1), where logic 0 input is 0 V and logic 1 input is 5 V (same for the below). (Inset) The output-input (V_o-V_i) relation. The solid and dashed red (blue) lines show V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). (**C**) The experimental truth table for the OR gate. (**D**) Schematic of logic AND gate constructed from a 1 by 3 crossed NW junction array. (Insets) A typical SEM (bar: 1 μm) of the assembled AND gate and symbolic electronic circuit. (**E**) The output voltage versus the four possible logic address level inputs. (Inset) The V_o-V_i, where the solid and dashed red (blue) lines correspond to V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). (**F**) The experimental truth table for the AND gate. (**G**) Schematic of logic NOR gate constructed from a 1 by 3 crossed NW junction array. (Insets) An example SEM (bar: 1 μm) and symbolic electronic circuit. (**H**) The output voltage versus the four possible logic address level inputs. (Inset) The V_o-V_i relation, where the solid and dashed red (blue) lines correspond to V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). The slope of the data shows that device voltage gain is larger than 5. (**I**) The measured truth table for the NOR gate.

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and arrays is especially important for integration without resorting to extensive top-down lithography to connect to those NT devices that function. Second, the use of crossed NW devices and arrays leads naturally to integration at the nanoscale and should be contrasted with NT (*3–5*, *8*) and molecular (*9–11*) devices, where the element sizes reported to date (length for NTs and area for molecules) have been determined by the same top-down lithography used in conventional electronics.

Lastly, we have interconnected multiple AND and NOR gates to implement basic computation in the form of an XOR gate (Fig. 3A), which corresponds to the binary logic function SUM, and a half adder (Fig. 3B), which corresponds to the addition of two binary bits. The XOR gate is configured by using the output from AND and NOR gates as the input to a second NOR gate, whereas the logic half adder uses an additional logic AND gate as the CARRY. The truth table for the proposed logic XOR is summarized in Fig. 3C. Importantly, the experimental V_o-V_i transport data for the XOR device (Fig. 3, D and E) show (i) that the output is logic state 0 or low when the inputs are both low or high, and logic state 1 or high when one input is low and the other is high; and (ii) that the response is highly nonlinear. The linear response region corresponds to a voltage gain of more than five and is typical of the devices measured to date. This large gain achieved in an XOR configured from CNW-FET NOR gates and a low-gain diode AND gate is due to the high gain of the cNW-FET NOR gates. We believe that further improvements in device performance could be obtained by using cNW-FET elements for all of the logic elements (*24*). Importantly, the data summarized in the experimental truth table (Fig. 3F) demonstrate that the response is that of the binary logic SUM operation, and thus that we have implemented a basic computation with the NW logic devices.

Overall, we believe that our predictable and reproducible bench-top assembly of nanoscale crossed p-n diode and cNW-FET elements and arrays, which have enabled the demonstration of all critical logic gates and basic computation, represents an important step toward integrated nanoelectronics built from primarily bottom-up versus top-down approaches. Further improvements can be made by assembling NWs directly onto predefined metal electrode arrays (*25*) and by creating more highly integrated circuit elements by feeding the output from NW to NW. Implementing these approaches could eliminate the conventional lithography used to wire-up devices in this study. In addition, in a crossbar array with 5-nm diameter NWs, it would be possible to achieve device densities approaching $10^{12}/cm^2$, which is off the present semiconductor road map for top-down manufacturing. To achieve this goal of bottom-up manufacturing in the future will require substantial work—for example, in developing much greater sophistication in assembly and further improving materials synthesis.

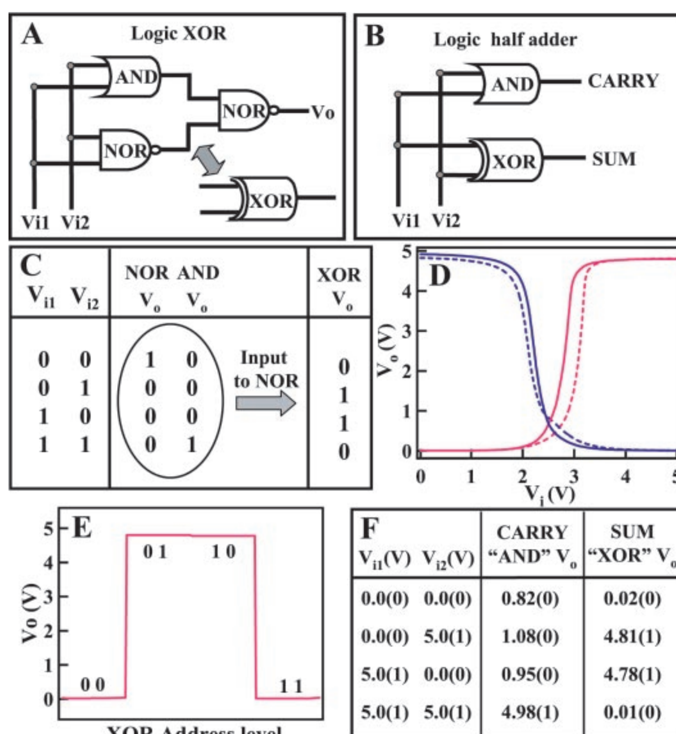

Fig. 3. Nanowire computation. (**A**) Schematic of logic XOR gate constructed with the output from an AND and a NOR as the input to a second NOR gate. (**B**) Schematic for logic half adder. (**C**) Truth table for logic XOR gate. (**D**) XOR output voltage versus input voltages. The solid and dashed red (blue) lines show V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). The slope of the V_o-V_i data shows that the gain exceeds 10. The XOR gate was achieved by connecting the output electrodes of an AND and NOR gate to two inputs of another NOR gate. (**E**) The output voltage versus the four possible logic address level inputs for the XOR gate. (**F**) Experimental truth table for the logic half adder. The logic half adder was obtained by using the XOR gate as the SUM and an AND gate as the CARRY.

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18. Single-crystal p-type Si-NWs were grown by using Au nanocluster catalysts, SiH_4 reactant, and B_2H_6 dopant (SiH_4:B_2H_6, 1000:1 to 6000:1) (*15*). Single-crystal GaN-NWs were prepared by a laser-assisted catalytic growth with iron as the catalyst (target composition: GaN:Fe = 95:5) (*17*) and are naturally n-type due to nitrogen vacancies or oxygen impurities (*26*). The SiNW surfaces consist of a ~1-nm-thick amorphous oxide, which can be removed by HF etching (*14*) or increased in thickness by thermal oxidation before device assembly. The GaN-NWs have only a monolayer-thick oxide over-layer (*27*), making them ideal for forming crossed NW junctions. Stable solutions of Si-NWs and GaN-NWs were prepared by sonication in ethanol for 5 to 10 s. Individual and multiple crossed NW junctions were prepared by using a layer-by-layer fluidic alignment strategy (*16*): First, Si-NWs were aligned on the Si/SiO_2 surface from the ethanol solution by using a microfluidic channel, and crossed GaN-NWs were deposited by using the microfluidic channel oriented perpendicular to the original SiNW flow. Au/Ti electrical contacts (50 nm Ti; 70 nm Au) to the nanowires were defined by electron-beam lithography and electron-beam evaporation.
19. *I-V* measurements made on individual p-Si and n-GaN NWs in crossed NW devices show linear *I-V* behavior. The p-Si NWs have two-terminal resistances of 0.5 to 10 megohms and were determined by the SiH_4:B_2H_6 ratio (1000:1 to 6000:1) used during growth. The n-GaN NWs have two-terminal resistances of 50 to 500 kilohms.
20. The turn-on voltages of crossed NW p-n junctions were increased by Joule heating the junctions in air. Because the crossing point dominates the junction resistance (*13*, *14*), a high current will locally heat the crossing point and increase the oxide layer between crossed NWs, and thereby the junction resistance/turn-on voltage. The red line in the top right inset of Fig. 1A shows the large change in turn-on voltage after passing a 10-μA current through the junction for about 4 min; the resistance changes of the individual NWs changed less than about 10%.
21. The cNW-FET on/off ratio can vary from 10^3 to 10^5, depending on the p-Si NW carrier concentration. In

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general, p-Si NWs grown with a higher dopant ratio (SiH_4:B_2H_6 = 1000:1) have lower resistance and smaller on/off ratios of $\sim 10^3$; those synthesized with a lower dopant ratio (6000:1) have higher resistance and larger on/off ratios of $\sim 10^4$ to 10^5. In addition, the carrier mobility typically varies from 30 to 200 cm^2/V-s, depending on doping.
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24. The OR and AND gates were assembled by using p-n junctions (diode logic) and do not exhibit voltage gain; however, they would show gain if implemented by using cNW-FETs. For example, logic OR can be implemented with the NOR gate by reversing the 5-V bias and ground connections to the p-Si NW. The AND function could also be implemented by using cNW-FETs in parallel (versus series for OR). In addition, we note that both p- and n-channel transistors are possible and would enable reduced power dissipation.
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Logic Circuits with Carbon Nanotube Transistors

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We demonstrate logic circuits with field-effect transistors based on single carbon nanotubes. Our device layout features local gates that provide excellent capacitive coupling between the gate and nanotube, enabling strong electrostatic doping of the nanotube from *p*-doping to *n*-doping and the study of the nonconventional long-range screening of charge along the one-dimensional nanotubes. The transistors show favorable device characteristics such as high gain (>10), a large on-off ratio (>10^5), and room-temperature operation. Importantly, the local-gate layout allows for integration of multiple devices on a single chip. Indeed, we demonstrate one-, two-, and three-transistor circuits that exhibit a range of digital logic operations, such as an inverter, a logic NOR, a static random-access memory cell, and an ac ring oscillator.

The anticipated limits to the further miniaturization of microelectronics have led to intense research directed toward the development of molecular electronics (*1*). The use of single-wall carbon nanotubes has stimulated these efforts, because these molecules exhibit a range of suitable properties for nanoelectronics. Various basic single-nanotube components have recently been demonstrated, such as molecular wires, diodes, field-effect transistors, and single-electron transistors (*2*–*8*). The next challenge in the development of molecular electronics is to go beyond single-molecule components and integrate such devices onto a chip to demonstrate digital logic operations. Here, we report such logic circuits composed of single-nanotube field-effect transistors. In addition to the realization of logic circuits, our new device layout also enables substantial electrostatic doping for modest gate voltages, which allows us to study the nonconventional screening of charge along the one-dimensional nanotubes.

Our nanotube transistors have a local gate that is insulated from the nanotube by a gate oxide layer of only a few nanometers thickness. In previous circuits, the gate consisted of an oxidized Si wafer (*6, 7, 9*), the tip of an atomic force microscope (*10*–*12*), a second nanotube (*13*), an ionic solution (*14*), or a capping Al film (*15*). The layouts of these devices do not allow integration of multiply connected devices (*16*). For example, the most popular nanotube-transistor layout uses a backgate, which applies the same gate voltage to all transistors on the chip. In contrast, our gate consists of a microfabricated Al wire with a well-insulating native Al_2O_3 layer (*17*), which lies beneath a semiconducting nanotube that is electrically contacted to two Au electrodes (Fig. 1, A and B). In this configuration, the Al_2O_3 thickness of a few nanometers is much shorter than the separation between the contact electrodes ($\sim$100 nm), enabling an excellent capacitive coupling between the gate and the nanotube. Moreover, different local Al gates can easily be patterned such that each one addresses a different nanotube transistor. This layout thus allows the integration of multiple nanotube field-effect transistors (FETs) on the same chip (Fig. 1C).

Our nanotube circuits are realized in a three-step process. First, Al gates are patterned using electron beam lithography (*18*) on an oxidized Si wafer. The insulating layer consists of the native oxide that grows by exposing the sample to air. The precise thickness of this layer is difficult to determine, but is on the order of a few nanometers (*19*). Second, single-wall carbon nanotubes produced by laser ablation are dispersed on the wafer from a dichloroethane suspension. With an atomic force microscope, those nanotubes are selected that have a diameter of about 1 nm and that are situated on top of the Al gate wires. Their coordinates are registered with respect to alignment markers. Finally, contact electrodes and interconnect wires are fabricated with electron-beam lithography by evaporating Au directly on the nanotube without an adhesion layer.

Very strong doping of the nanotube channel can be achieved with this layout (Fig. 2A) (*20*). Starting from a negative gate voltage V_g, the current *I* first decreases, then becomes immeasurably small, and finally increases again. This indicates that V_g shifts the Fermi level successively from the valence band (accumulation regime) to the gap (depletion), and finally to the conduction band (inversion) of the semiconducting nanotube. The nearby Al gate thus makes it possible to change the doping of the nanotube over the full range from the *p*- to the *n*-doped regime.

Our nanotube transistors can be classified as enhancement-mode *p*-type FETs (*21*), because a strong modulation of the current through the nanotube FET is possible when a small negative gate voltage is applied. The current versus bias voltage V_{sd} characteristics (Fig. 3) are typical for FETs (*22*). From the data in Figs. 2 and 3, we can extract a transconductance of our nanotube transistors of 0.3 μS and a lower limit of the on/off ratio of at least 10^5. The maximum current at which the nanotube transistor can operate is on the order of 100 nA and the on-resistance is 26 megaohms for $V_{sd} = -1.3$ V and $V_g = -1.3$ V.

For any further development of operational logic circuits, a gain (>1) at large bias voltage is a crucial requirement, because the output of one logic structure must be able to drive the input of the next logic structure. The output typically has to provide a voltage swing of about 1 V. Figure 3 indicates that in our transistors, a change in the output by more than 1 V occurs when the input voltage is changed by 0.1 V. This indicates a large-signal gain >10. A large gain combined with a large output swing can be obtained because the gate is so close to the nanotube. Our technique allows for a much larger gain than has been achieved with thick gate oxides or planar gates used in previous nanotube FETs (*6, 7, 9, 23*).

A major point of our report is that small circuits combining our nanotube transistors can be used for a variety of logic elements. Here, we describe our demonstration of an inverter, a

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Emerging nanoscale silicon devices taking advantage of nanostructure physics

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This paper describes the present status of research on emerging nanoscale silicon devices that take full advantage of new physical phenomena which appear in silicon nanostructures. This new physics includes quantum effects that enhance the performance of MOS transistors and single-electron charging effects that add new function to conventional CMOS circuits. These physical phenomena may be used to extend the scaling and performance limits of conventional CMOS.

Introduction

The silicon MOSFET for very large scale integration (VLSI) has been scaled down for more than thirty years to attain higher levels of integration and higher performance. Recently, the miniaturization rate has accelerated, and the gate length is now less than 40 nm. These silicon devices are certainly in the nanometer regime. Further miniaturization of silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) into nanoscale complementary MOS (CMOS) will significantly affect advances in future information technology. **Figure 1** shows future gate lengths and technology nodes as projected in the 2003 version of the International Technology Roadmap for Semiconductors (ITRS) [1]. The roadmap predicts that gate lengths in mass-produced CMOS transistors will be less than 10 nm in the year 2016.

At the research level, on the other hand, a 40-nm n-MOS was reported in 1993 [2], and smaller devices followed [3–6]. Finally, in 2003, CMOS devices with gate lengths of 5 nm were reported [7]. These gate lengths are also included in Figure 1. It appears from the figure that a result first reported in research takes more than ten years to go into production. Many technical barriers to the realization of sub-10-nm CMOS devices still remain.

It is now well recognized that a simple scaling of bulk MOSFETs will fail in the nanometer regime. New techniques to overcome the scaling and performance limits of conventional CMOS devices are urgently needed. One of the most promising techniques is the utilization of new physical phenomena that appear in silicon nanostructures but have not yet been utilized in nanoscale devices. This paper describes the present status of silicon nanoscale devices that take full advantage of nanostructure physics. It is suggested that there are three stages in the research of silicon nanoscale devices. It is then demonstrated that the first two stages are particularly important for the future development of nanoscale devices for large-scale integration. Note that we are discussing nanoscale devices for integration rather than discrete devices. We also focus on the mainstream information processing device technologies including memories, instead of specific devices for niche applications.

Three stages in nanoscale silicon devices

Silicon devices will certainly be miniaturized. Then, new physical phenomena, such as quantum effects and single-electron charging effects, will occur even at room temperature in these devices. The VLSI device designers have avoided these physical phenomena in nanoscale structures for a long time because the effects sometimes cause unfavorable leakage current and device characteristic fluctuations. However, new physical phenomena will definitely appear in future nanodevices. Moreover, new functionalities that arise because of these phenomena have a huge potential for practical use in information processing or data storage. These new effects in nanoscale structures should be intensively studied and positively utilized for future integrated devices.

There are three stages in silicon nanodevices that positively utilize the new physics in nanoscale structures depending on how the physical phenomena are utilized in devices and how the devices are applied to integrated circuits.

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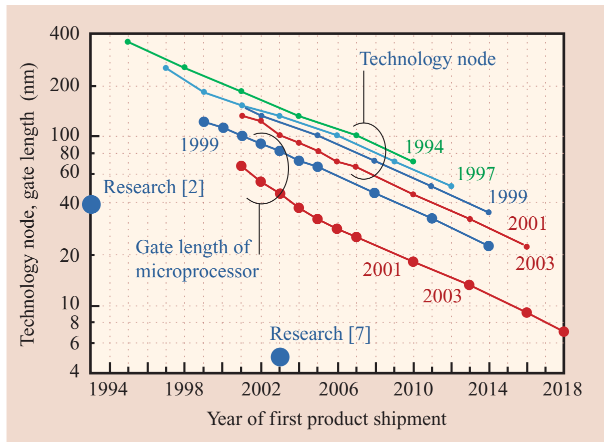

Figure 1

Prediction of gate length of MOSFETs in high-performance (HP) microprocessors by ITRS [1]. Technology nodes predicted by the 1994–2003 versions of ITRS and gate lengths predicted by the 1999–2003 versions of ITRS are plotted. The predictions of the 2001 version and the 2003 version are the same. Devices reported in research are also shown [2, 7].

- First stage: The basic operating principle of the nanoscale devices is conventional CMOS, but new physical phenomena in nanodevices enhance the performance of nano-CMOS.
- Second stage: New function appears in the nanoscale devices by new physics, and the devices are merged into CMOS circuits to add new functionalities. The operations are still based on CMOS.
- Third stage: The nanoscale devices operate by new physics, and these devices operating by new principles are integrated to form new circuits. The circuits are no longer CMOS.

In the first stage of development, the performance of CMOS is enhanced by new physical phenomena that include quantum effects and ballistic transport in nanoscale devices. Since the present CMOS platform need not be changed for system design and manufacturing, the first stage will come in the nearest future. In the middle of the first stage, a paradigm shift may take place from top-down-type nanodevices (fabricated by lithography and etching) to bottom-up-type nanodevices (formed by a self-assembly process). If the operating principle of a device fabricated by the bottom-up process is the same as for conventional CMOS, this device is classified into the second half of the first stage. For example, carbon nanotube (CNT) FETs, formed by the bottom-up process, are classified into the second half of the first stage if the integrated CNT-FETs form CMOS circuits. The second half of the first stage is not described in detail in this paper.

The second stage of development adds new functionalities in CMOS. The last half of the first stage and the second stage will overlap in time, and they will compete for the development of future integrated devices. At both the first and second stages, the life of CMOS will be prolonged, and these stages will have a great impact on the future development of CMOS and all information technologies.

At the third stage, however, the circuits are no longer CMOS, and completely new types of nanoscale devices, such as spin transistors, will be integrated. Then, the system architecture will not be the same as the conventional one. Therefore, in the present authors' opinion, the third stage will be realized as a mainstream device technology only in the distant future; the first two stages are of much more importance for current developments. Actual examples of technologies pertaining to the first and second stages are described in the following sections.

First stage: Enhancing performance

If new physics can enhance the performance of CMOS, it will exceed the performance limit and scaling limit of CMOS. For example, the performance of nanoscale CMOS devices can actually be controlled and improved by the quantum confinement effect. By experiments and simulation [8–11], we have investigated the characteristics of nanoscale narrow-channel MOSFETs and nanoscale thin-channel MOSFETS on silicon-on-insulator (SOI) substrates, where the carriers are respectively confined into a one-dimensional narrow channel and a two-dimensional thin channel.

Confinement into nanoscale narrow channel

Figure 2(a) shows a SEM image of a fabricated nanoscale narrow channel [8]. The channel width is less than 10 nm. In the nanoscale narrow channel, the carriers are confined in a one-dimensional channel, and the confinement is stronger than in a thin, planar channel. Therefore, more evidence of quantum effects is expected. It has been experimentally confirmed that the threshold voltage of narrow MOSFETs is varied and controlled depending on the channel width because the ground energy of carriers is raised by quantum confinement [8, 9].

It is also shown by simulation that the mobility is modified in nanoscale narrow-channel MOSFETs [9]. **Figure 2(b)** shows the ratio of mobility of [100]-oriented narrow-channel MOSFETs to that of [110]-oriented devices as a function of channel width. Conventional MOSFETs have the channel in the [110] direction, and the [100] direction is rotated from the [110] direction by 45 degrees. This larger mobility in [100]-oriented devices

is due to the anisotropic effective mass of silicon. In an n-type MOSFET, this mobility enhancement is explained by the electron population of valleys in the conduction band.

Figure 2(c) shows the conduction-band structure in [110]- and [100]-oriented channels. Owing to the anisotropy of the electron mass, the rise of valley energy is different depending on the direction of the ultranarrow channel. In the [110]-oriented ultranarrow channel, six equivalent valleys split into two sets of valleys: twofold degenerate valleys and fourfold degenerate valleys. When the channel width becomes narrower, the energy of the twofold degenerate valleys increases more than that of the fourfold degenerate valleys; therefore, more electrons are populated in the latter. However, fourfold degenerate valleys have larger mass and smaller mobility along the [110] direction than twofold degenerate valleys, as shown in Figure 2(c). Accordingly, the total electron mobility of [110]-oriented narrow-channel MOSFETs is smaller [9].

In the [100]-oriented narrow channel, on the other hand, six equivalent valleys split into three sets of twofold degenerate valleys, as shown in Figure 2(c). Most of the electrons are populated in the valley shown in red because the energy of this valley is the smallest, and this valley has the smallest mass and the highest mobility. For this reason, [100]-oriented narrow-channel MOSFETs have higher total mobility than [110]-oriented narrow-channel MOSFETs [9]. This performance enhancement is scalable because when the device becomes smaller, more quantum confinement takes place and mobility is increased.

Confinement into nanoscale thin channel

In nanoscale thin-channel devices, the confinement of carriers is weak compared with the confinement into nanoscale narrow channels because the carriers can have two degrees of freedom. Moreover, the transport properties in a two-dimensional electron gas of a quantum well in silicon [12] or in GaAs [13] have already been investigated in detail at very low temperatures. However, we have found experimentally that the hole mobility is largely enhanced in an ultrathin-channel silicon-on-insulator (SOI) MOSFET at room temperature due to quantum confinement when the substrate crystal orientation is (110) [10, 11]. This is one of the best examples of the first stage.

Figure 3(a) shows a schematic structure of fabricated SOI p-MOS devices [10]. The crystal orientation of silicon on the buried oxide, or SOI, is (110) and the channel direction is [110]. The silicon thickness is in the range of 3 nm. The TEM images of the gate oxide/silicon/buried oxide from fabricated devices are shown in **Figure 3(b)**. The silicon thickness of the source and drain regions is kept thicker by using a local oxidation technique in order to make the parasitic resistance negligible. **Figure 4(a)** shows the measured hole mobility as a function of silicon

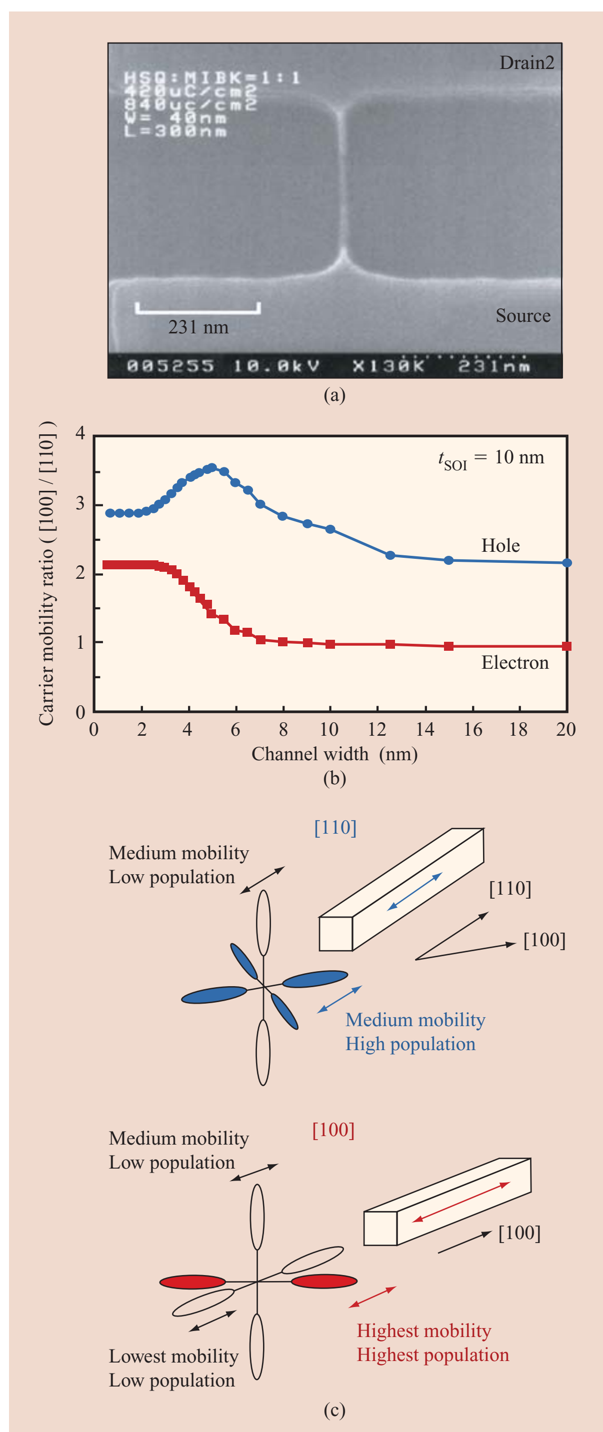

Figure 2

(a) SEM image of nanoscale narrow channel. The narrow channel with width of less than 10 nm is formed between source and drain. Adapted from [8] with permission; ©2000 IEEE. (b) Simulated mobility ratio of [100]-oriented channel to [110]-oriented channel as a function of channel width. (c) Conduction band structure in [110]-oriented and [100]-oriented nanoscale narrow channels. Parts (b) and (c) adapted from [9] with permission; ©2001 IEEE.

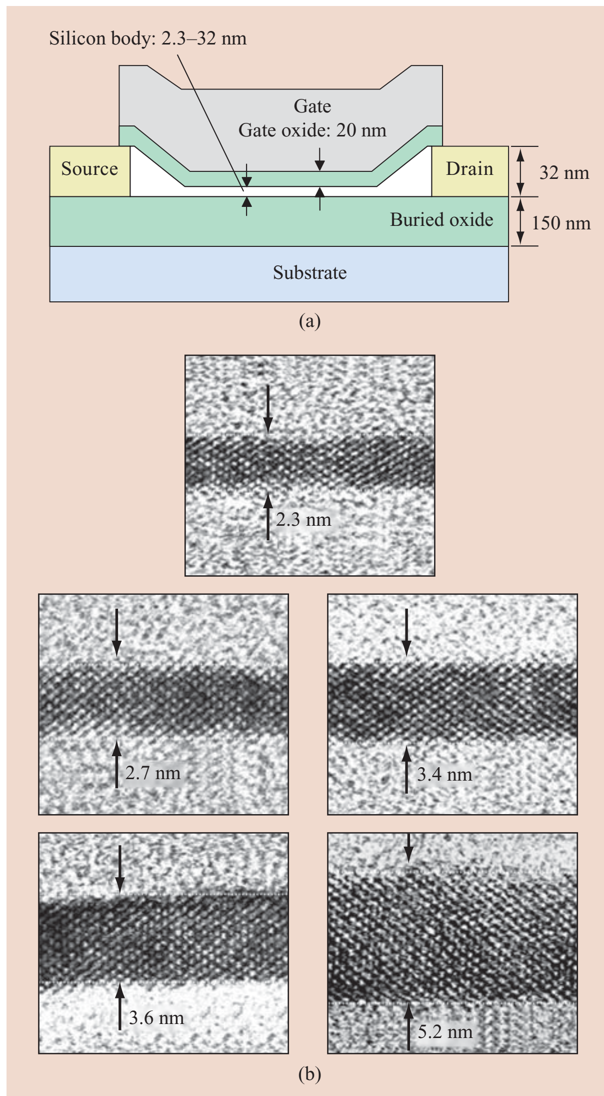

Figure 3

(a) Schematic of (110)-oriented ultrathin-body SOI p-MOS devices. (b) TEM images of measured ultrathin-body p-MOS devices. Adapted from [10] with permission; ©2005 IEEE.

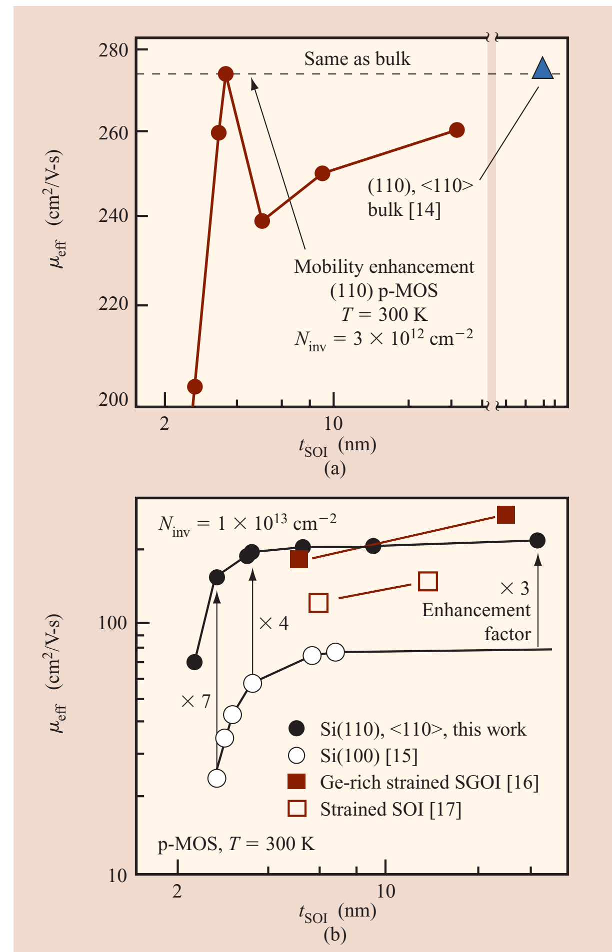

Figure 4

Measured hole mobility of (110) p-MOSFETs as a function of SOI thickness at room temperature. (a) Hole mobility at inversion carrier density of 3×10^{12} cm^{-2}. The mobility in a bulk (110) p-MOSFET is also shown [14]. (b) Hole mobility at inversion carrier density of 1×10^{13} cm^{-2}. Mobility data for other p-MOSFETs is also shown [15–17]. The enhancement factors compared with those for Si(100) p-MOSFETs are shown. Adapted from [11] with permission; ©2005 IEEE.

thickness at room temperature at an inversion carrier density of 3×10^{12} cm^{-2} [11]. As the narrow-channel silicon becomes thinner, the hole mobility decreases because of increased acoustic phonon scattering. However, a clear mobility enhancement is observed at thicknesses of 3.4 and 3.6 nm. The peak mobility is almost the same as the mobility in bulk (110) p-MOSFETs [14]. This phenomenon is explained by the suppression of inter-subband phonon scattering assisted by optical phonon absorption that is the transition between the two lowest-lying heavy-hole subbands [11]. Note that the increase in hole mobility is observed only in (110) ultrathin-body p-MOS and not in (100) because of the high degree of degeneracy of heavy and light holes.

Figure 4(b) shows measured hole mobility as a function of SOI thickness at room temperature at an inversion carrier density of 1×10^{13} cm^{-2}, where the density is higher than in Figure 4(a) and is more important for practical use [11]. The (110) p-MOSFETs retain high mobility even when the body thickness is thinned down to 3 nm, and the mobility is higher than that of other devices, including Si (110) bulk [15], Ge-rich strained SiGe on insulator (SGOI) [16], and strained SOI p-MOSFETs [17] at a thickness of less than 6 nm. In this thin-body regime, the dominant

scattering mechanism is the scattering induced by SOI thickness fluctuation [15]. The high mobility in (110) p-MOSFETs in the extremely thin-body regime is explained by the suppression of the SOI-thickness-fluctuation-induced scattering compared with that in conventional (100) p-MOSFETs [11]. This is because the (110) p-MOSFET is less sensitive to SOI-thickness-fluctuation-induced scattering due to heavier hole effective mass normal to the channel surface, as predicted in [18]. In the nanoscale CMOS, the crystal orientation, channel direction, and device dimension should be carefully determined in order to maximize the device performance.

Second stage: New functions merged into CMOS

Memory

In the second stage, new functionalities that appear are merged into CMOS. The best example of the second stage is a memory chip, which is composed of memory cell arrays that store digital data and peripheral circuits that write and read the data. In a new memory, nanostructures can be adopted and new functions can be utilized only in the memory cells, while conventional CMOS devices are utilized in the peripheral circuits. Therefore, all of the research work on new and nanoscale memory devices is classified into the second stage.

We have demonstrated a new function in silicon nanocrystal memories [19, 20], where silicon nanocrystals are embedded in gate oxide and act as sites for charge storages. Physical separation of nanocrystals can improve the retention time by limiting the lateral flow of charges. The new function that appears in a silicon nanocrystal memory cell is the two-bit-per-cell operation [21]. The electrons are locally injected only near drain and/or source by hot-carrier injection, and there are four states depending on where the electrons are injected. Distinct four-threshold voltages are experimentally observed that can be read out [21].

Single-electron transistor

A single-electron transistor [22, 23] is one of the best-known nanoscale devices. The single-electron transistor has a unique feature of Coulomb blockade oscillations in *I–V* characteristics, and therefore has great potential to add new functionalities to future VLSI. Although many circuit applications of single-electron transistors have been proposed so far, these applications are unfortunately classified into the third stage, in which new devices with new principles are integrated to form new circuits that are no longer CMOS. If the single-electron transistor is in the second stage, it has more potential to be realized as a new functional device in the near future. Therefore, a new application of a single-electron transistor in the second stage is strongly required.

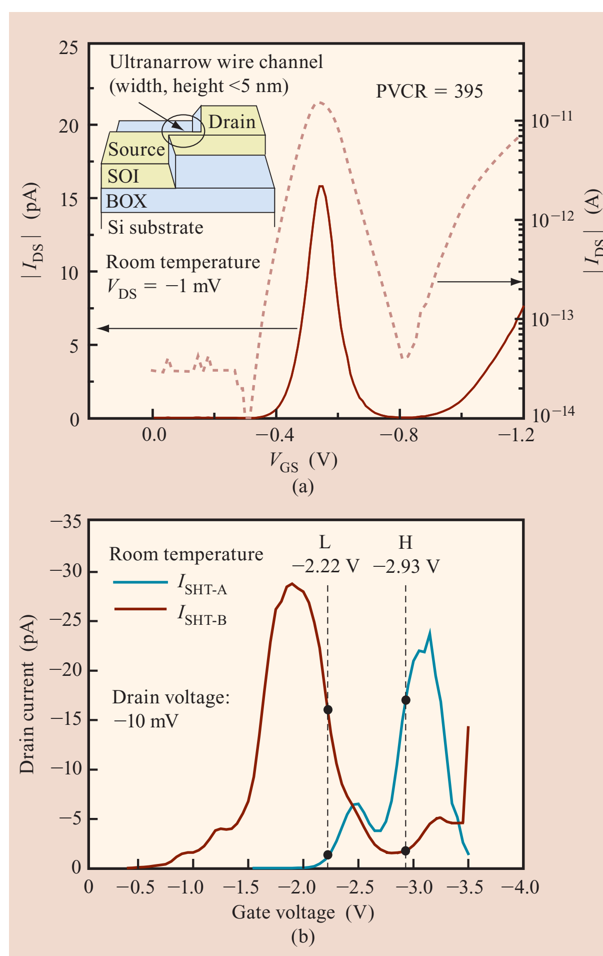

Figure 5

(a) Coulomb blockade oscillations of a single-hole transistor at room temperature. The device structure is shown in the inset. Adapted from [25] with permission; ©2004 IEEE. (b) Characteristics of two integrated room-temperature-operating single-hole transistors. A directional current switch operation is successfully demonstrated. Adapted from [27] with permission.

Our single-electron/hole transistor is in the form of a point-contact MOSFET. The silicon quantum dot is self-formed in the very narrow channel, and the device acts as a single-electron/hole transistor [24]. Some single-electron/hole transistors are in the form of an ultranarrow-channel MOSFET, as shown in the inset of **Figure 5(a)**. Single-electron/hole transistors generally operate only at very low temperature, and great efforts have been made to raise the operation temperature by making the silicon quantum dot smaller. Figure 5(a) shows the *I–V* characteristics of a single-hole transistor at room temperature [25]. This example shows the largest Coulomb blockade oscillations in a single-dot system ever reported at room temperature. The peak-to-valley current

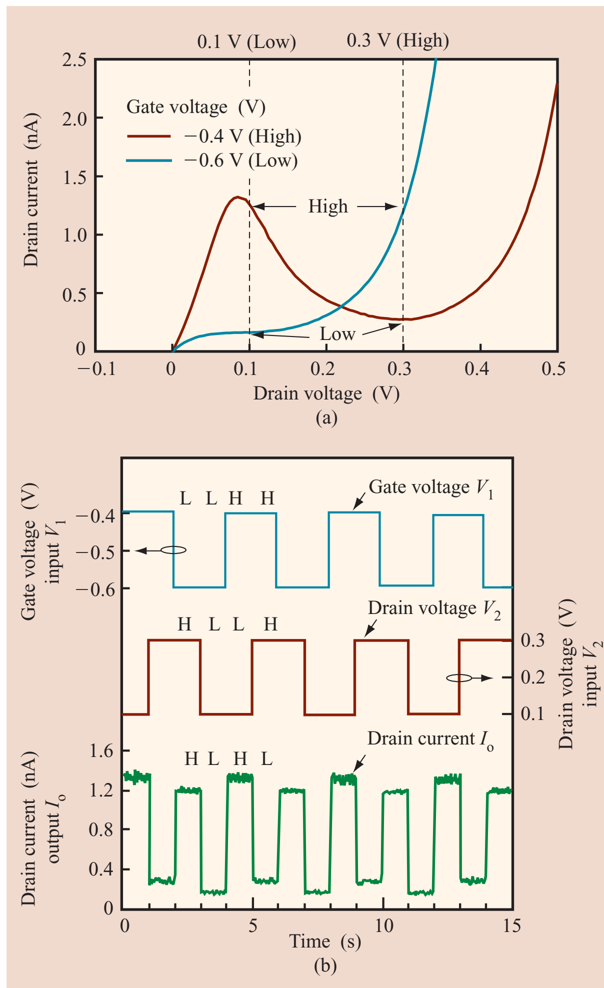

Figure 6

(a) Characteristics of a single-hole transistor that exhibits NDC at room temperature. (Please note that the horizontal axis is drain voltage, not gate voltage.) (b) Operation of exclusive-OR function by only one single-hole transistor at room temperature. Adapted from [29] with permission.

ratio (PVCR) is as large as 395; the estimated dot size is as small as 2 nm. Since the dot is extremely small, the quantum-level spacing in the dot is not negligible, and negative differential conductance (NDC) due to resonant tunneling, which also has new functionality, is observed at room temperature [25, 26]. The PVCR of NDC is as large as 106 at room temperature.

Efforts have been made to integrate room-temperature-operating single-electron/hole transistors. **Figure 5(b)** shows Coulomb blockade oscillations of two integrated single-hole transistors that form a directional current switch at room temperature [27]. This is the first integration of the room-temperature-operating single-electron/hole transistors. Moreover, each single-hole transistor has silicon nanocrystals embedded in the gate oxide and acts as a nonvolatile memory. Therefore, the peak position of Coulomb blockade oscillations can be controlled by applying gate pulse voltage that injects electrons into silicon nanocrystals [28]. This adds a new function to single-electron/hole transistors.

A concrete example of single-electron/hole transistors in the second stage is a digital circuit application. If a part of conventional CMOS circuits is replaced by single-electron/hole transistors, new functions are added with extremely low power consumption. **Figure 6(a)** shows characteristics of an exclusive-OR circuit. The circuit is composed of only one single-hole transistor that exhibits NDC at room temperature [29]. The modulation of NDC characteristics by gate voltage is utilized. When the gate voltage and drain voltage are inputs of the circuit, the output current shows the exclusive-OR function, as shown in **Figure 6(b)**. Compared with the conventional exclusive-OR circuit by CMOS, the number of devices is greatly reduced when the single-electron/hole transistor is used because of its high functionality.

Another application of single-electron/hole transistors in the second stage is analog circuit application. The bell-shaped *I–V* characteristics can be utilized for the analog pattern matching circuits [30]. Since the Coulomb blockade oscillations have bell-shaped *I–V* characteristics, we have applied them to analog pattern matching [28]. In this application, the matching is performed by the single-hole transistors, and other calculations are done by conventional CMOS circuits. Therefore, this new circuit scheme utilizing single-electron/hole transistors and adding new function to CMOS is in the second stage.

Conclusion

The present status of the research on silicon nanoscale devices is described. It is suggested that there are three stages in the nanoscale silicon devices, and that the utilization of new physical phenomena observed in nanostructures may prolong the extendability of CMOS devices. Successful applications of the physical phenomena described are expected to overcome the present performance and scaling limits of CMOS.

Acknowledgments

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